

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSQF06N70H-C is power MOSFET using Super Junction Technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of low EMI to designers as well as low switching loss, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSQF06N70H-C meet the RoHS and Green Product requirement with full function reliability approved.

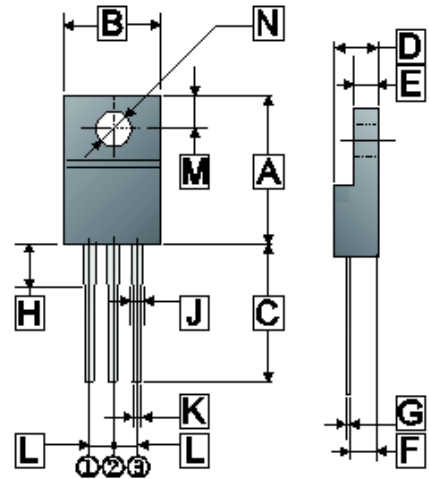
FEATURES

- Advanced Super Junction Technology
- Super Low Gate Charge
- Green Device Available

MARKING



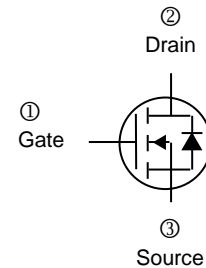
ITO-220J



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	14.8	15.2	H	2.2 REF.	
B	9.96	10.36	J	0.9 REF.	
C	13.20 REF.		K	0.5	0.75
D	4.35	4.65	L	2.54 REF.	
E	2.85	3.15	M	2.70 REF.	
F	2.60	2.80	N	ϕ 3.5 REF.	
G	0.50	0.75			

ORDER INFORMATION

Part Number	Type
SSQF06N70H-C	Lead (Pb)-free and Halogen-free



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	700	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ¹ @ $V_{GS}=10\text{V}$	I_D	$T_C=25^\circ\text{C}$	6
		$T_C=100^\circ\text{C}$	4
Pulsed Drain Current ³	I_{DM}	26	A
Total Power Dissipation	P_D	36.7	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Ratings			
Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Thermal Resistance Junction-Ambient ²		110	
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	3.4	

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Drain-Source Breakdown Voltage	BV_{DSS}	700	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	2	-	4	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 30\text{V}$	
Drain-Source Leakage Current	I_{DSS}	$T_J=25^\circ\text{C}$	-	-	1	μA	$V_{DS}=560\text{V}, V_{GS}=0$
		$T_J=55^\circ\text{C}$	-	-	5		
Static Drain-Source On-Resistance ⁴	$R_{DS(ON)}$	-	0.58	0.65	Ω	$V_{GS}=10\text{V}, I_D=2.1\text{A}$	
Total Gate Charge	Q_g	-	23	-	nC	$I_D=6\text{A}$ $V_{DS}=560\text{V}$ $V_{GS}=10\text{V}$	
Gate-Source Charge	Q_{gs}	-	4.3	-			
Gate-Drain ("Miller") Charge	Q_{gd}	-	11.2	-			
Turn-on Delay Time	$T_{d(on)}$	-	14.4	-	nS	$V_{DD}=350\text{V}$ $I_D=6\text{A}$ $V_{GS}=10\text{V}$ $R_G=25\Omega$	
Rise Time	T_r	-	27.6	-			
Turn-off Delay Time	$T_{d(off)}$	-	68	-			
Fall Time	T_f	-	26	-			
Input Capacitance	C_{iss}	-	681	-	pF	$V_{GS}=0\text{V}$ $V_{DS}=25\text{V}$ $f=1\text{MHz}$	
Output Capacitance	C_{oss}	-	450	-			
Reverse Transfer Capacitance	C_{rss}	-	32.6	-			
Source-Drain Diode							
Diode Forward Voltage ⁴	V_{SD}	-	-	1.4	V	$I_S=6\text{A}, V_{GS}=0\text{V}$	
Continuous Source Current ¹	I_S	-	-	6	A	$V_G=V_D=0, \text{Force Current}$	
Pulsed Source Current ³	I_{SM}	-	-	26	A		
Reverse Recovery Time	T_{rr}	-	344	-	nS	$V_{DD}=100\text{V}, I_S=6\text{A},$ $di/dt=100\text{A}/\mu\text{s}$	
Reverse Recovery Charge	Q_{rr}	-	4.3	-	μC		

Notes:

1. Surface mounted on a 1 inch² FR-4 board with 2oz copper.
2. When mounted on Min. copper pad.
3. Pulse width limited by maximum junction temperature, pulse width $\leq 10\mu\text{s}$, duty cycle $\leq 2\%$.
4. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS CURVE

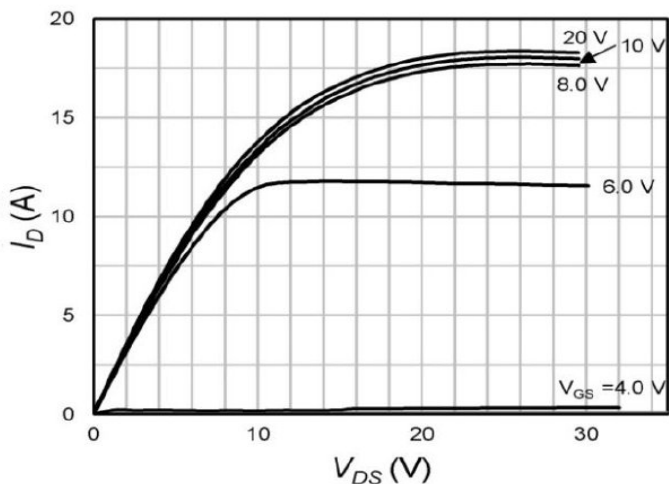


Fig.1 Typical Output Characteristics

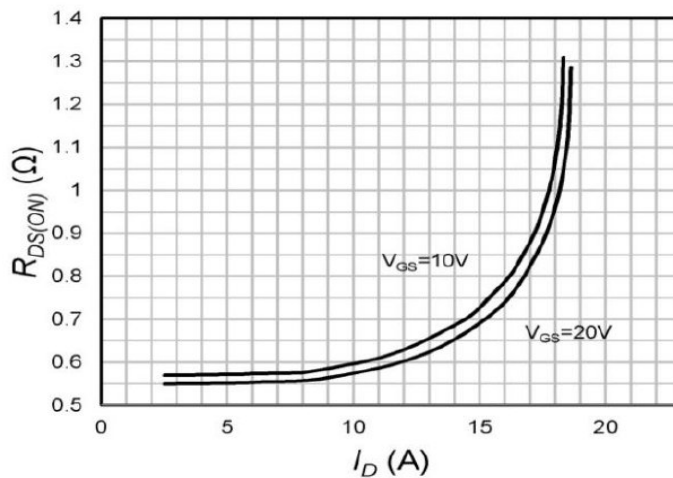


Fig.2 On-Resistance vs. Drain Current

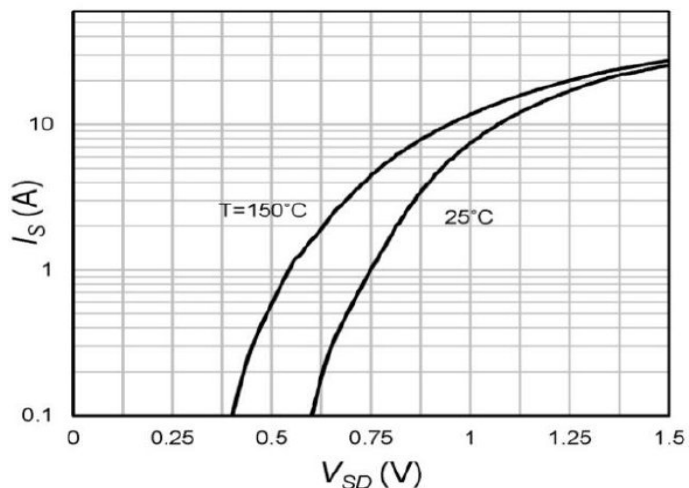


Fig.3 Forward Characteristics of Reverse

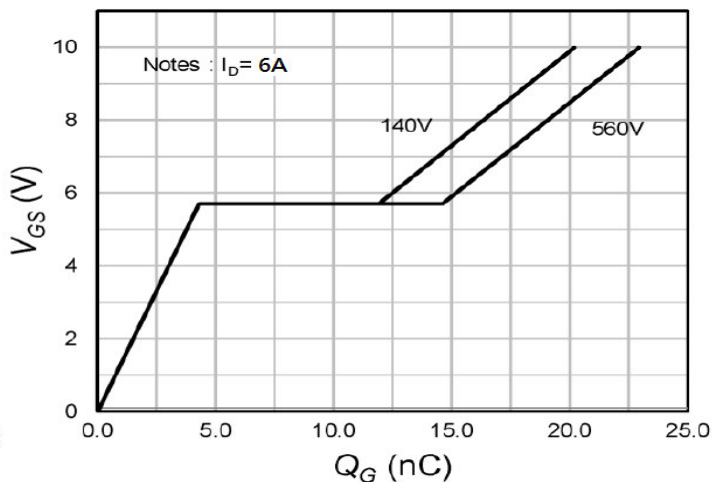


Fig.4 Gate-Charge Characteristics

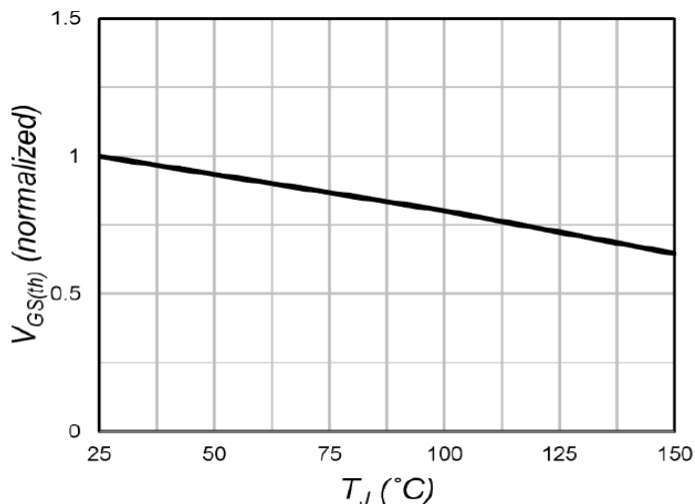


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

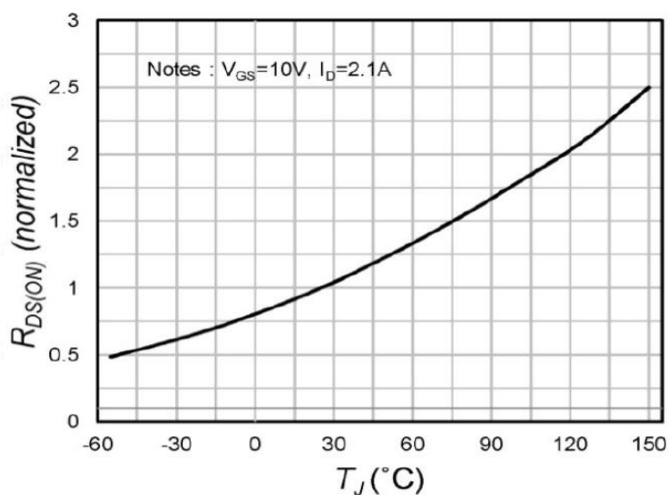


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

TYPICAL CHARACTERISTICS CURVE

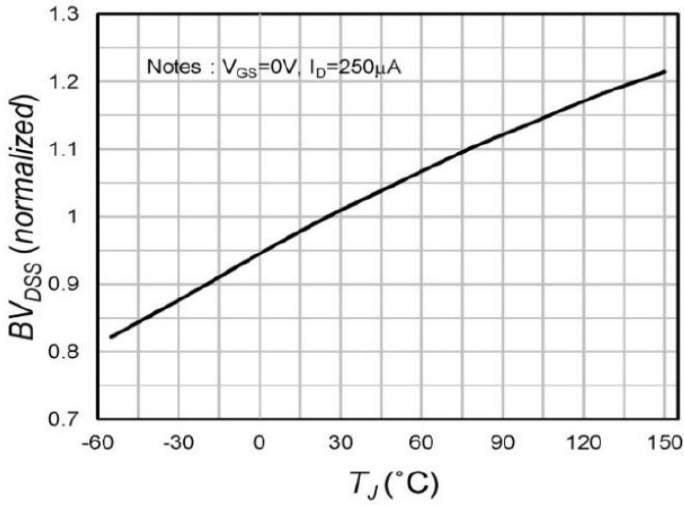


Fig.7 Drain-Source Breakdown Voltage(Normaized)

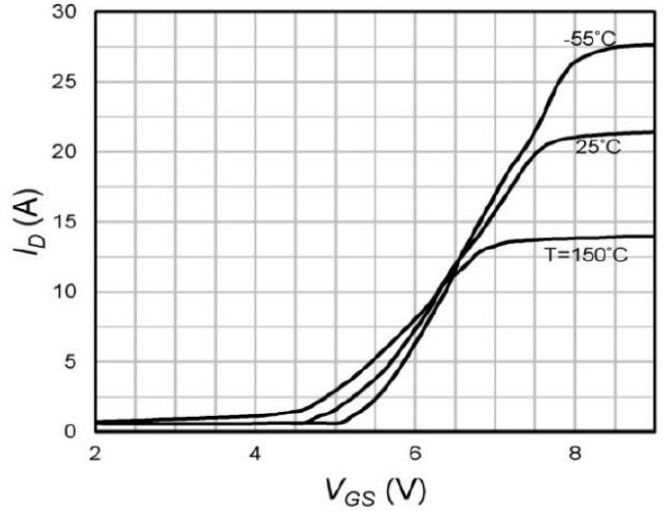


Fig.8 Transfer Characteristics

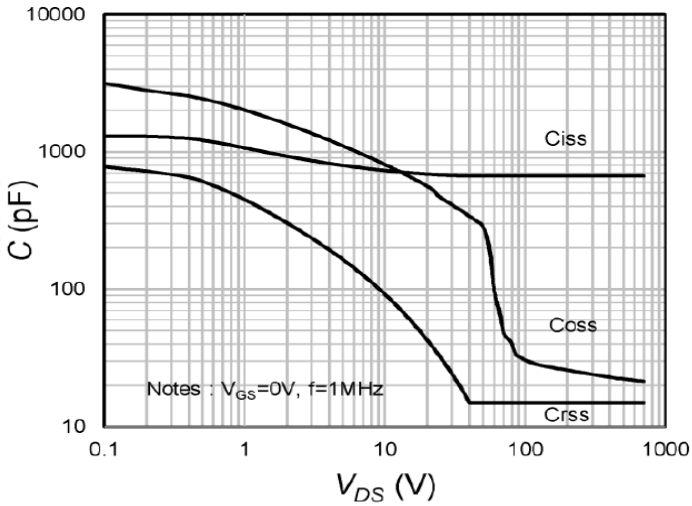


Fig.9 Capacitances

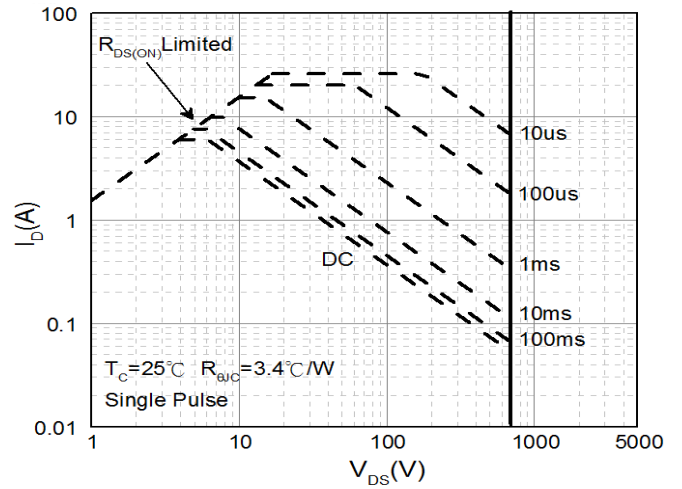


Fig.10 Safe Operating Area

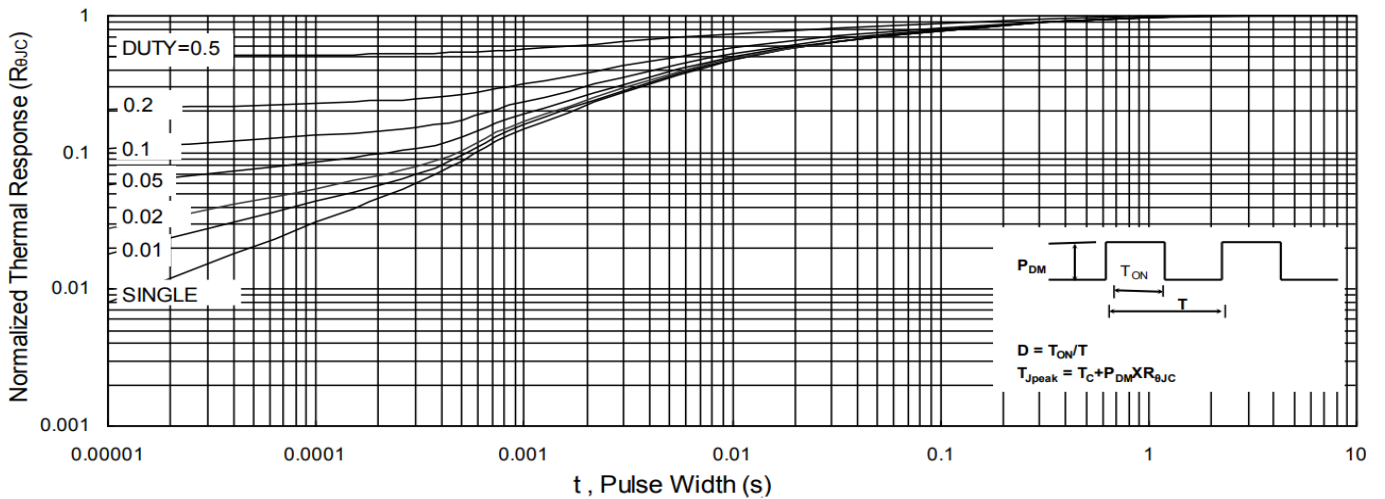


Fig.11 Normalized Maximum Transient Thermal Impedance