

RoHS Compliant Product
 A suffix of "-C" specifies halogen free

DESCRIPTION

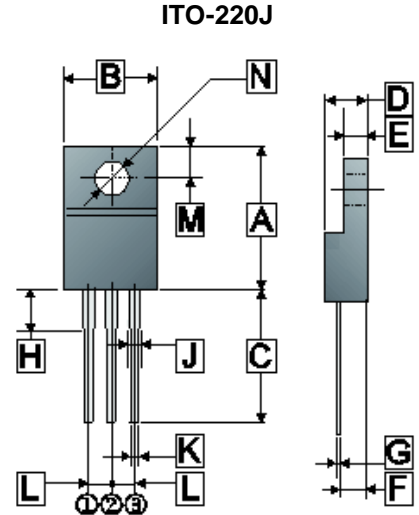
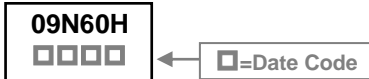
The SSQF09N60H-C is power MOSFET using Super Junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of low EMI to designers as well as low switching loss, which provide excellent R_{DS(ON)} and gate charge for most of the synchronous buck converter applications.

The SSQF09N60H-C meet the RoHS and Green Product requirement with full function reliability approved.

FEATURES

- Advanced Super Junction technology
- Super Low Gate Charge
- Green Device Available

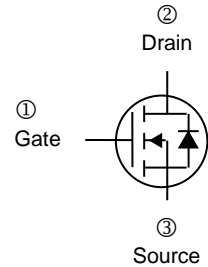
MARKING



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	14.8	15.2	H	2.2	REF.
B	9.96	10.36	J	0.9	REF.
C	13.20	REF.	K	0.5	0.75
D	4.35	4.65	L	2.54	REF.
E	2.85	3.15	M	2.70	REF.
F	2.60	2.80	N	φ 3.5	REF.
G	0.50	0.75			

ORDER INFORMATION

Part Number	Type
SSQF09N60H-C	Lead (Pb)-free and Halogen-free



ABSOLUTE MAXIMUM RATINGS (T_J=25°C unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V _{DS}	600	V
Gate-Source Voltage	V _{GS}	±30	V
Continuous Drain Current ⁵ (Silicon Limited)	I _D	T _C =25°C	13.8
		T _C =100°C	8.7
Continuous Drain Current ¹ (Package Limited)	I _D	T _C =25°C	9.5
		T _C =100°C	6
Pulsed Drain Current ³	I _{DM}	42	A
Total Power Dissipation	P _D	34.7	W
Operating Junction & Storage Temperature Range	T _J , T _{STG}	-55~150	°C
Thermal Resistance Ratings			
Thermal Resistance Junction-Ambient ¹	R _{θJA}	62.5	°C/W
Thermal Resistance Junction-Ambient ²		110	
Thermal Resistance Junction-Case ¹	R _{θJC}	3.6	

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Drain-Source Breakdown Voltage	BV_{DSS}	600	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	2	-	4	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 30\text{V}$	
Drain-Source Leakage Current	I_{DSS}	$T_J=25^\circ\text{C}$	-	-	1	μA	$V_{DS}=480\text{V}, V_{GS}=0$
		$T_J=55^\circ\text{C}$	-	-	5		
Static Drain-Source On-Resistance ⁴	$R_{DS(ON)}$	-	0.25	0.28	Ω	$V_{GS}=10\text{V}, I_D=6\text{A}$	
Total Gate Charge	Q_g	-	25	-	nC	$I_D=9\text{A}$ $V_{DD}=480\text{V}$ $V_{GS}=10\text{V}$	
Gate-Source Charge	Q_{gs}	-	7	-			
Gate-Drain ("Miller") Charge	Q_{gd}	-	9	-			
Turn-on Delay Time	$T_{d(on)}$	-	20	-	nS	$V_{DS}=300\text{V}$ $I_D=9\text{A}$ $V_{GS}=10\text{V}$ $R_G=25\Omega$	
Rise Time	T_r	-	43	-			
Turn-off Delay Time	$T_{d(off)}$	-	91	-			
Fall Time	T_f	-	42	-			
Input Capacitance	C_{iss}	-	941	-	pF	$V_{GS}=0$ $V_{DS}=25\text{V}$ $f=1\text{MHz}$	
Output Capacitance	C_{oss}	-	927	-			
Reverse Transfer Capacitance	C_{rss}	-	42	-			
Source-Drain Diode							
Diode Forward Voltage ⁴	V_{SD}	-	-	1.4	V	$I_S=9\text{A}, V_{GS}=0\text{V}$	
Continuous Source Current ¹	I_S	-	-	9.5	A		
Pulsed Source Current ³	I_{SM}	-	-	42	A		
Reverse Recovery Time	T_{rr}	-	364	-	nS	$V_{DD}=100\text{V}, I_S=9\text{A},$ $di/dt=100\text{A}/\mu\text{s}$	
Reverse Recovery Charge	Q_{rr}	-	4.7	-	nC		

Notes:

1. Surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. When mounted on Min. copper pad.
3. Pulse width limited by maximum junction temperature, pulse width $\leq 10\mu\text{s}$, duty cycle $\leq 2\%$.
4. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
5. I_D limited by maximum junction temperature.

TYPICAL CHARACTERISTICS CURVE

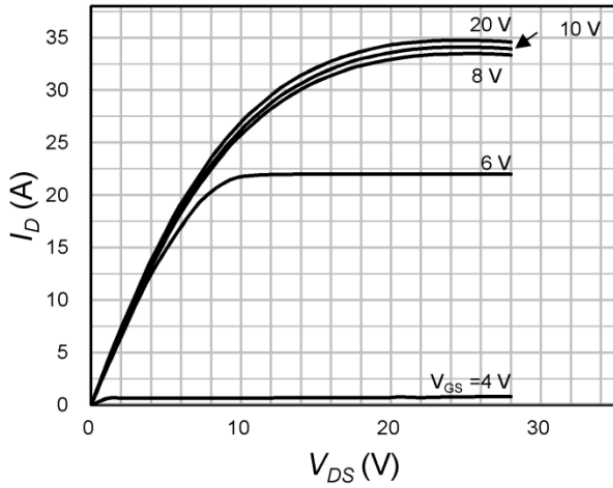


Fig.1 Typical Output Characteristics

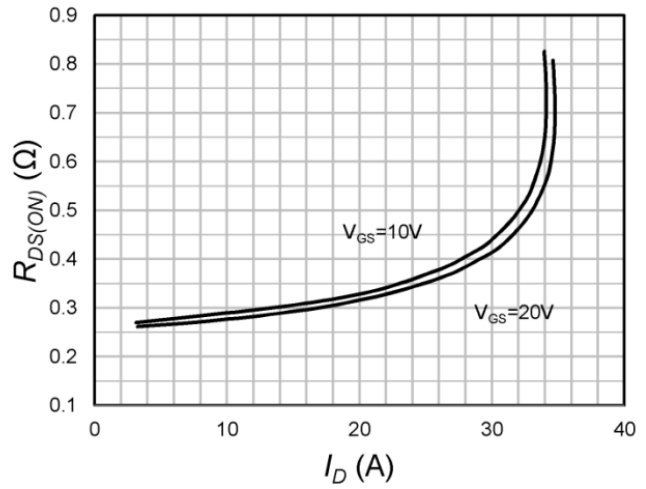


Fig.2 On-Resistance vs. Drain Current

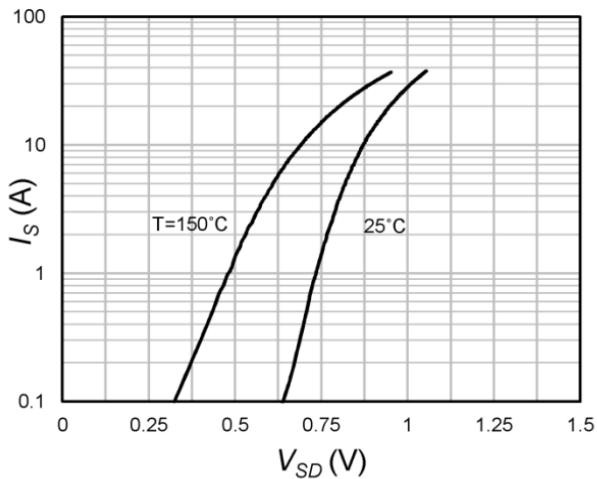


Fig.3 Forward Characteristics of Reverse

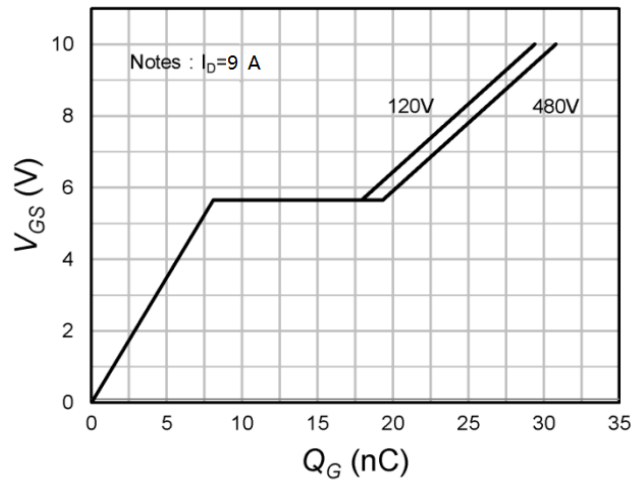


Fig.4 Gate-Charge Characteristics

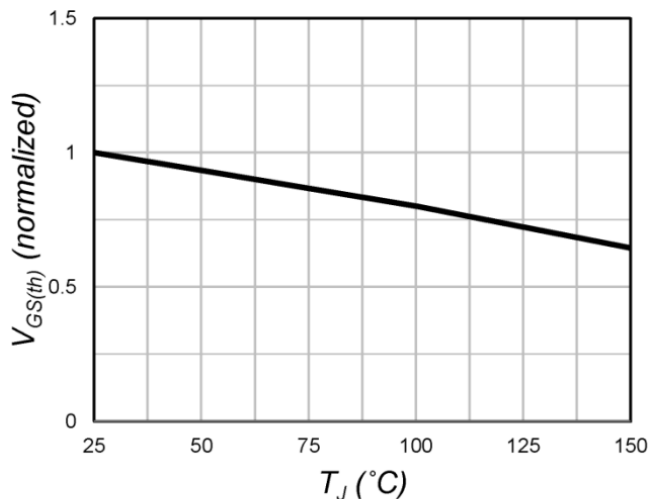


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

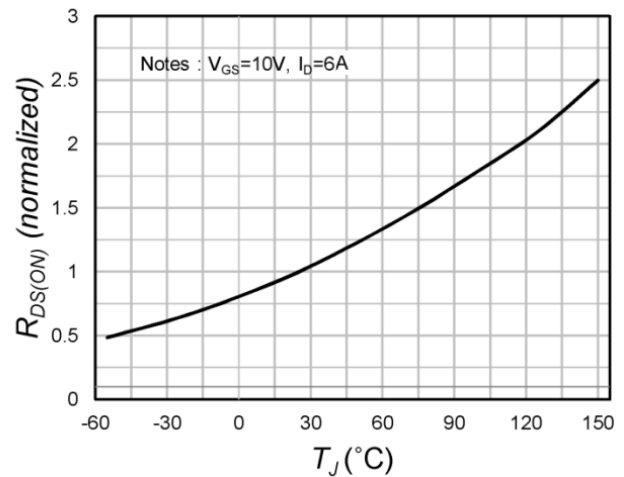


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

TYPICAL CHARACTERISTICS CURVE

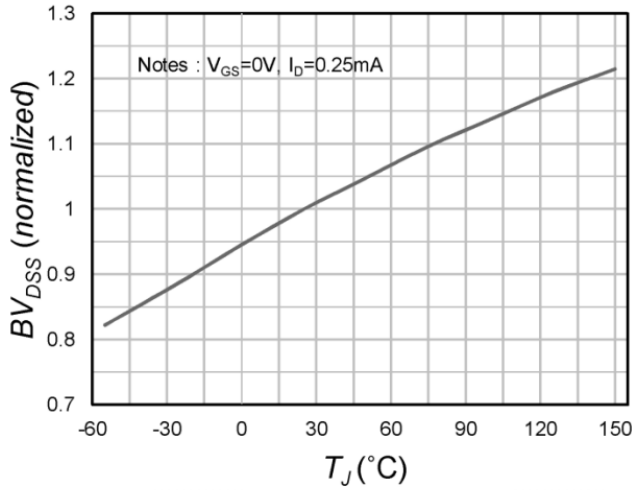


Fig.7 Drain-Source Breakdown Voltage(Normaized)

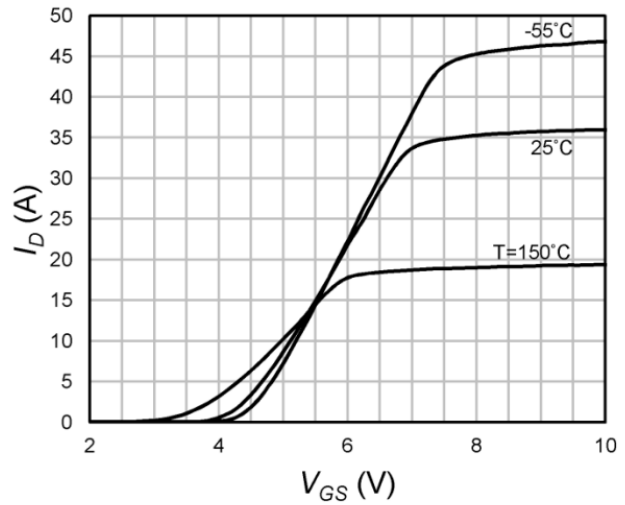


Fig.8 Transfer Characteristics

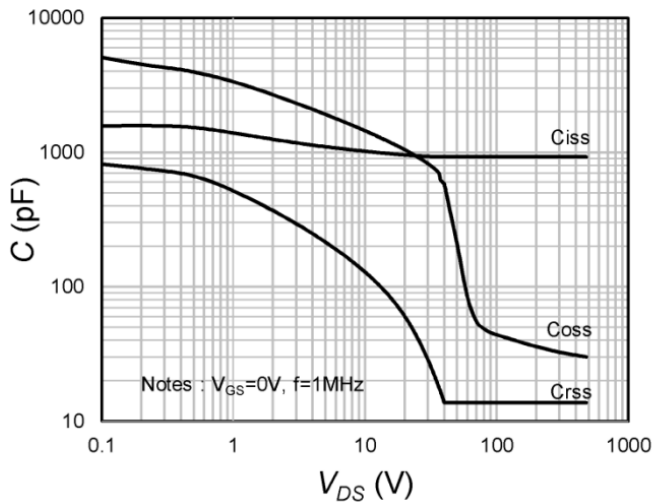


Fig.9 Capacitances

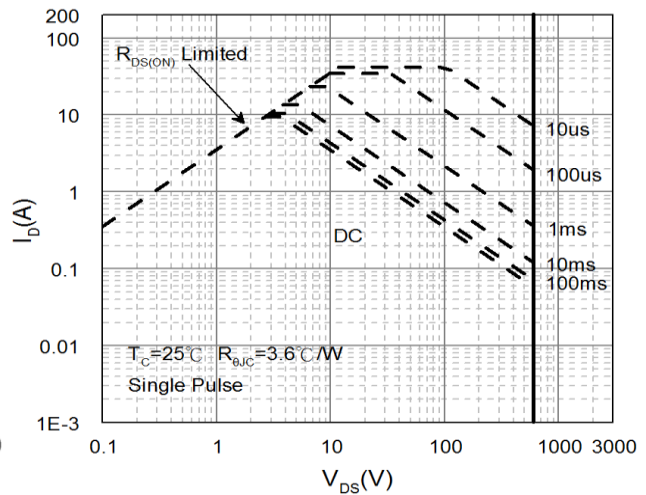


Fig.10 Safe Operating Area

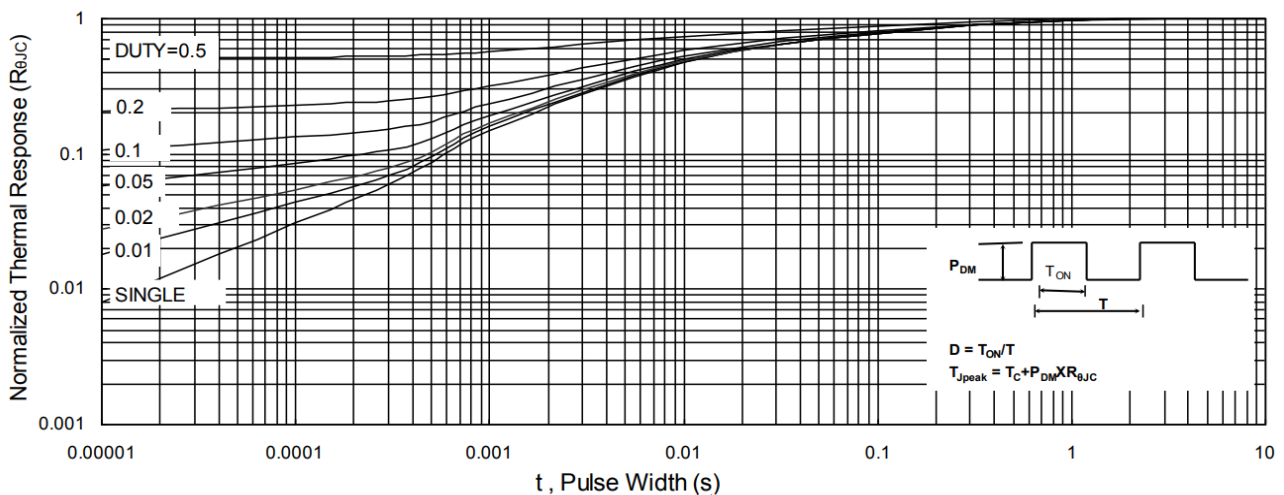


Fig.11 Normalized Maximum Transient Thermal Impedance