

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

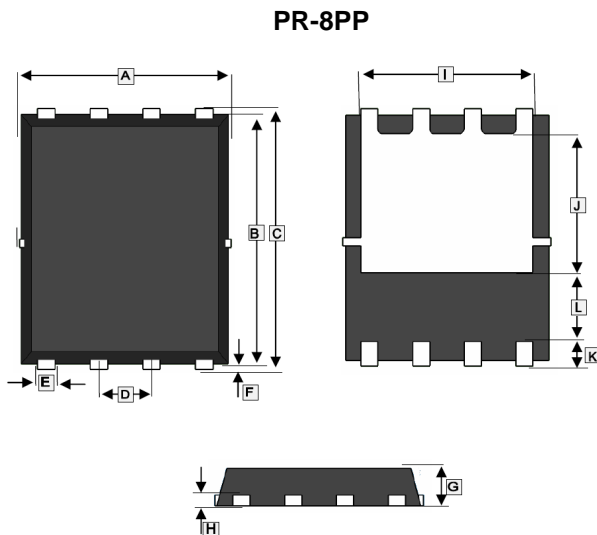
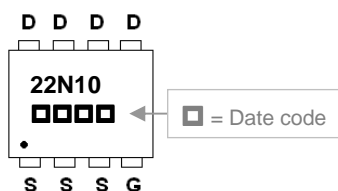
DESCRIPTION

The SPR22N10 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The PR-8PP package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

FEATURES

- Lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic

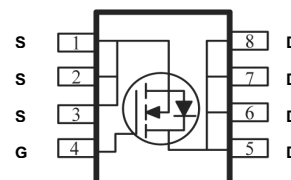
MARKING



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.9	5.1	G	0.8	1.0
B	5.7	5.9	H	0.254 Ref.	
C	5.95	6.2	I	4.0 Ref.	
D	1.27 BSC.		J	3.4 Ref.	
E	0.35	0.49	K	0.6 Ref.	
F	0.1	0.2	L	1.4 Ref.	

PACKAGE INFORMATION

Package	MPQ	Leader Size
PR-8PP	3K	13 inch



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current ¹ @V _{GS} =10V	I _D	T _C =25°C	22
		T _C =100°C	13.5
Pulsed Drain Current ²	I _{DM}	45	A
Single Pulse Avalanche Energy ³	EAS	26.6	mJ
Avalanche Current	I _{AS}	20	A
Total Power Dissipation ⁴	P _D	52.1	W
Operating Junction & Storage Temperature	T _J , T _{STG}	-55~150	°C
Thermal Resistance Rating			
Thermal Resistance Junction-Ambient ¹ (Max).	R _{θJA}	36	°C / W
Thermal Resistance Junction-Case ¹ (Max).	R _{θJC}	2.4	°C / W

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	100	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Forward Transconductance	g_{fs}	-	28.7	-	S	$V_{DS}=5\text{V}, I_D=20\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{V}$
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	$V_{DS}=80\text{V}, V_{GS}=0, T_J=25^\circ\text{C}$
		-	-	100		$V_{DS}=80\text{V}, V_{GS}=0, T_J=55^\circ\text{C}$
Static Drain-Source On-Resistance ²	$R_{DS(ON)}$	-	38	48	m Ω	$V_{GS}=10\text{V}, I_D=20\text{A}$
		-	40	50		$V_{GS}=4.5\text{V}, I_D=15\text{A}$
Gate Resistance	R_g	-	1.6	3.2	Ω	$f=1.0\text{MHz}$
Total Gate Charge	Q_g	-	60	-	nC	$I_D=20\text{A}$ $V_{DS}=80\text{V}$ $V_{GS}=10\text{V}$
Gate-Source Charge	Q_{gs}	-	9.7	-		
Gate-Drain ("Miller") Charge	Q_{gd}	-	11.8	-		
Turn-on Delay Time ²	$T_{d(on)}$	-	10.4	-	nS	$V_{DD}=50\text{V}$ $I_D=20\text{A}$ $V_{GS}=10\text{V}$ $R_G=3.3\Omega$
Rise Time	T_r	-	46	-		
Turn-off Delay Time	$T_{d(off)}$	-	54	-		
Fall Time	T_f	-	10	-		
Input Capacitance	C_{iss}	-	3848	-	pF	$V_{GS}=0$ $V_{DS}=15\text{V}$ $f=1.0\text{MHz}$
Output Capacitance	C_{oss}	-	137	-		
Reverse Transfer Capacitance	C_{rss}	-	82	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy ⁵	EAS	6	-	-	mJ	$V_{DD}=25\text{V}, L=0.1\text{mH}, I_{AS}=10\text{A}$
Source-Drain Diode						
Diode Forward Voltage ²	V_{SD}	-	-	1.2	V	$I_S=1\text{A}, V_{GS}=0\text{V}$
Continuous Source Current ^{1,6}	I_S	-	-	22	A	$V_G=V_D=0$, Force Current
Pulsed Source Current ^{2,6}	I_{SM}	-	-	45	A	
Reverse Recovery Time	t_{rr}	-	30	-	nS	$I_F=20\text{A}, dI/dt=100\text{A}/\mu\text{s},$ $T_J=25^\circ\text{C}$
Reverse Recovery Charge	Q_{rr}	-	37	-	nC	

Note:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper , $\leq 10\text{sec}$, $125^\circ\text{C}/\text{W}$ at steady state
- The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating . The test condition is $V_{DD}=25\text{V}, V_{GS}=10\text{V}, L=0.1\text{mH}, I_{AS}=20\text{A}$
- The power dissipation is limited by 150°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

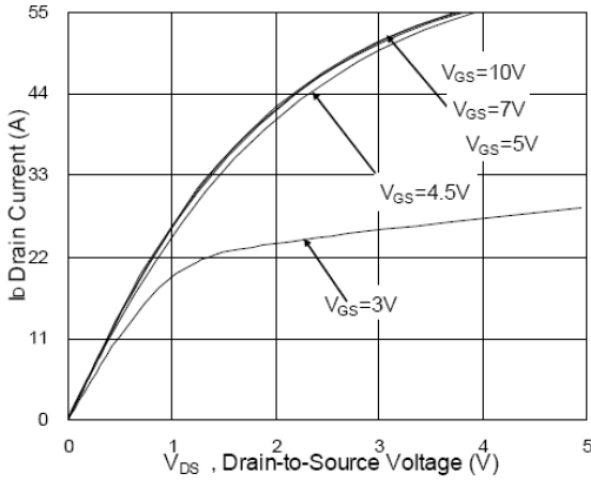


Fig.1 Typical Output Characteristics

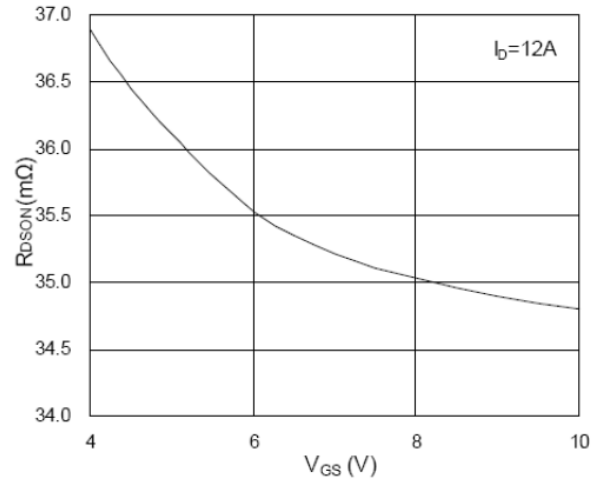


Fig.2 On-Resistance vs. Gate-Source

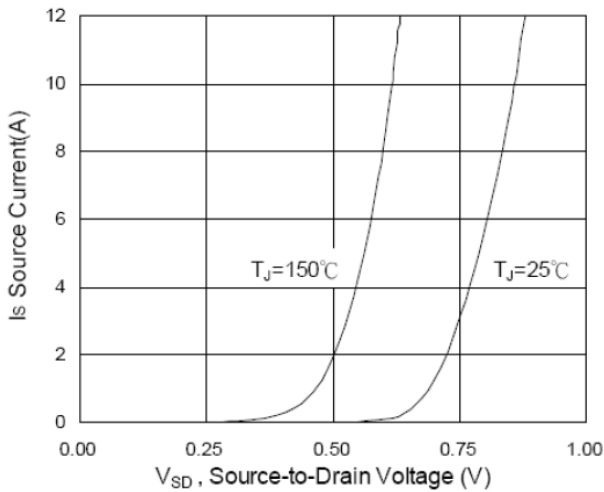


Fig.3 Forward Characteristics Of Reverse

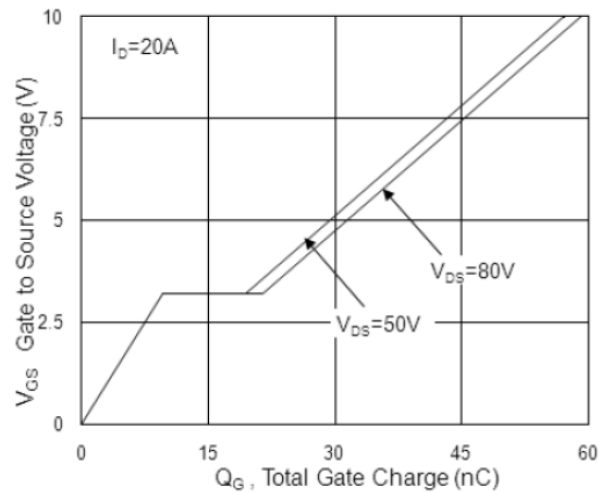


Fig.4 Gate-Charge Characteristics

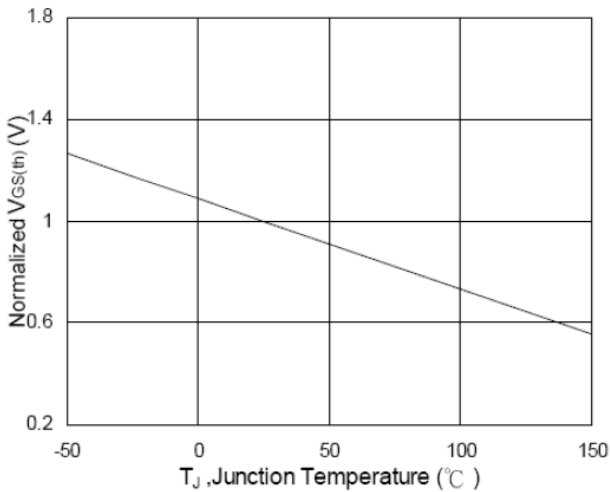


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

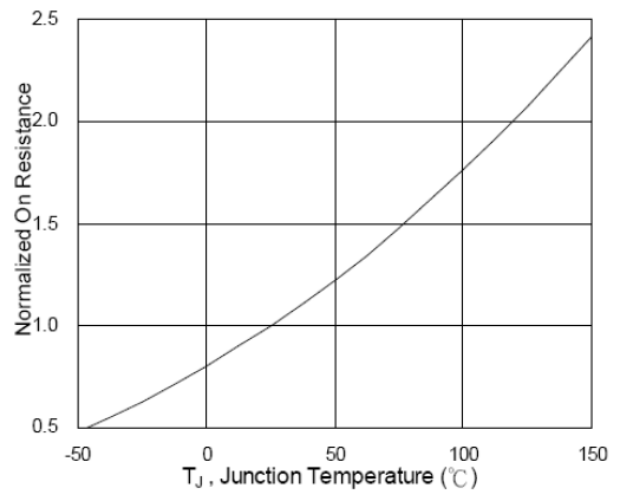


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

CHARACTERISTIC CURVES

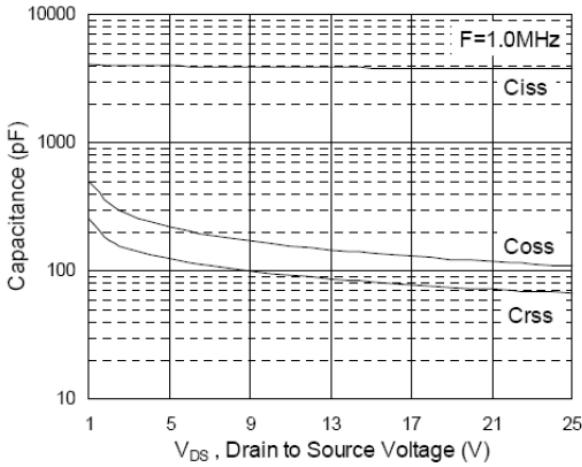


Fig.7 Capacitance

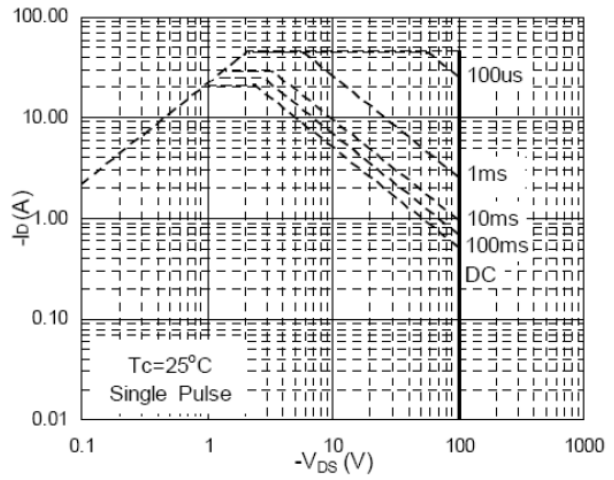


Fig.8 Safe Operating Area

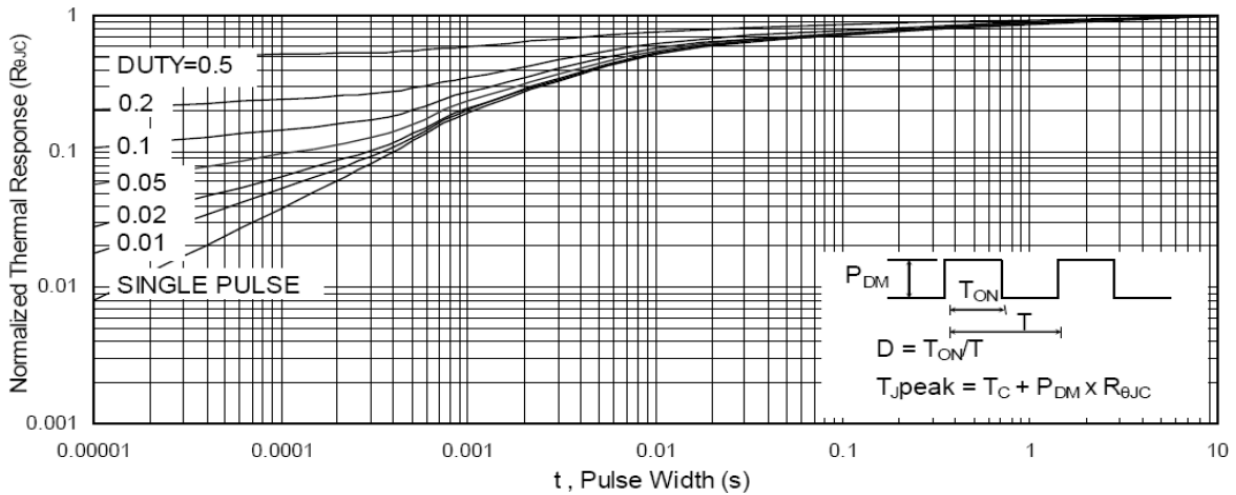


Fig.9 Normalized Maximum Transient Thermal Impedance

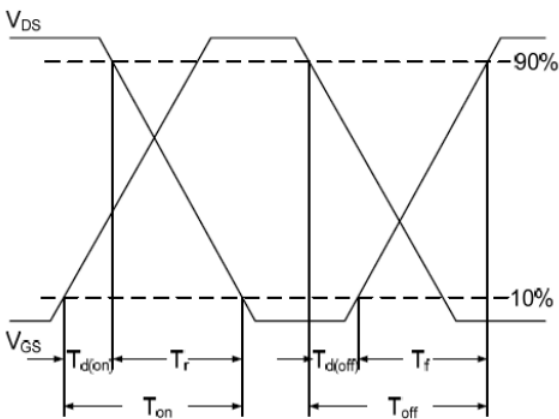


Fig.10 Switching Time Waveform

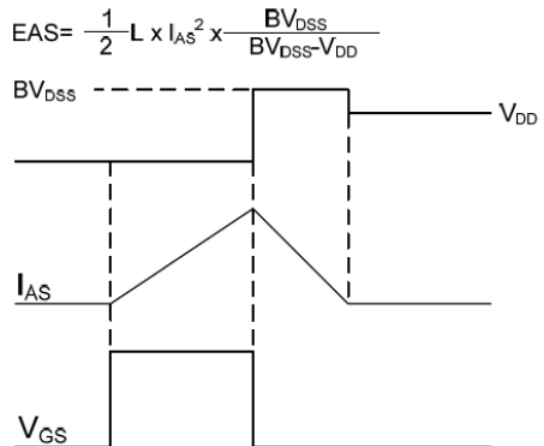


Fig.11 Unclamped Inductive Switching Waveform