

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

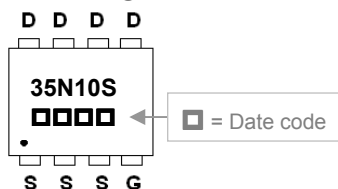
The SPR35N10S-C is the highest performance trench N-Ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SPR35N10S-C meet the RoHS and Green Product requirement with full function reliability approved.

FEATURES

- Lower Gate Charge
- Advanced high cell density Trench technology
- Green Device Available

MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
PR-8PP	3K	13 inch

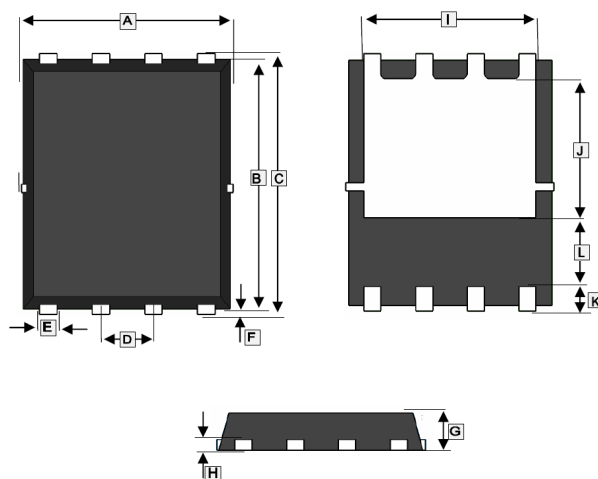
ORDER INFORMATION

Part Number	Type
SPR35N10S-C	Lead (Pb)-free and Halogen-free

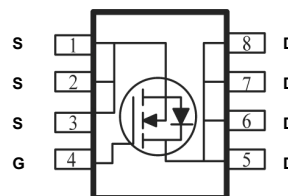
ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹ (Silicon Limited)	I_D	$T_C=25^\circ\text{C}$	35
		$T_C=100^\circ\text{C}$	25
Continuous Drain Current ¹ (Package Limited)	$T_C=25^\circ\text{C}$	28	A
Pulsed Drain Current ^{2,4}	I_{DM}	180	A
Power Dissipation	P_D	31	W
Operating Junction & Storage Temperature	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Ratings			
Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	55	$^\circ\text{C/W}$
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	4	

PR-8PP



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.9	5.1	G	0.8	1.0
B	5.7	5.9	H	0.254	Ref.
C	5.95	6.2	I	4.0	Ref.
D	1.27 BSC		J	3.4	Ref.
E	0.35	0.49	K	0.6	Ref.
F	0.1	0.2	L	1.4	Ref.



ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0V, I_D=250\mu A$	
Gate-Threshold Voltage	$V_{GS(th)}$	1.4	-	2.4	V	$V_{DS}=V_{GS}, I_D=250\mu A$	
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$	
Drain-Source Leakage Current	I_{DSS}	-	-	1	uA	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ\text{C}$	
		-	-	100		$V_{DS}=80V, V_{GS}=0V, T_J=100^\circ\text{C}$	
Static Drain-Source On-Resistance ³	$R_{DS(ON)}$	-	14	17	m Ω	$V_{GS}=10V, I_D=15A$	
		-	22	26		$V_{GS}=4.5V, I_D=10A$	
Transconductance	g_{fs}	-	42	-	S	$V_{DS}=5V, I_D=15A$	
Gate Resistance	R_g	-	1.6	-	Ω	$V_{DS}=V_{GS}=0V, f=1\text{MHz}$	
Total Gate Charge (4.5V)	Q_g	-	9	-	nC	$I_D=15A$ $V_{DD}=50V$ $V_{GS}=10V$	
Total Gate Charge		-	16	-			
Gate-Source Charge		Q_{gs}	-	3			-
Gate-Drain Change		Q_{gd}	-	3			-
Turn-on Delay Time	$T_{d(on)}$	-	6	-	nS	$V_{DD}=50V$ $I_D=15A$ $V_{GS}=10V$ $R_G=10\Omega$	
Rise Time	T_r	-	3	-			
Turn-off Delay Time	$T_{d(off)}$	-	13	-			
Fall Time	T_f	-	3	-			
Input Capacitance	C_{iss}	-	840	-	pF	$V_{GS}=0V$ $V_{DS}=50V$ $f=1\text{MHz}$	
Output Capacitance	C_{oss}	-	147	-			
Reverse Transfer Capacitance	C_{rss}	-	4.9	-			
Source-Drain Diode							
Diode Forward Voltage ³	V_{SD}	-	-	1.2	V	$I_F=20A, V_{GS}=0V$	
Reverse Recovery Time	T_{rr}	-	30	-	nS	$I_F=15A, V_R=50V, di/dt=500A/\mu s$	
Reverse Recovery Charge	Q_{rr}	-	105	-	nC		

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The Pulse width limited by maximum junction temperature, Pulse Width $\leq 10\mu s$, Duty Cycle $\leq 2\%$
3. The Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
4. Package limit.

CHARACTERISTIC CURVES

Fig 1. Typical Output Characteristics

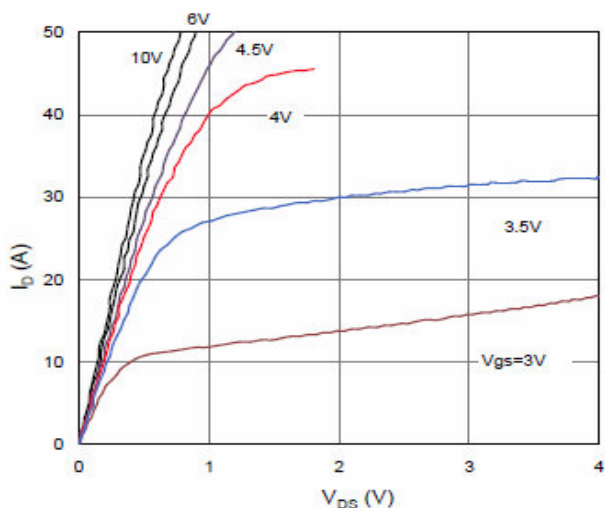


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

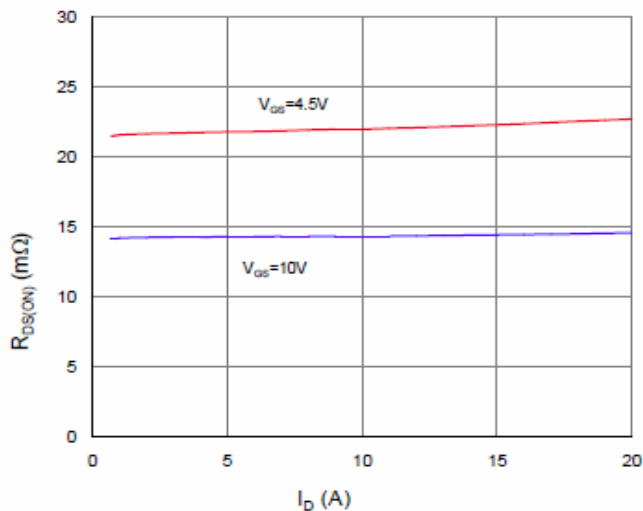


Figure 5. Typical Transfer Characteristics

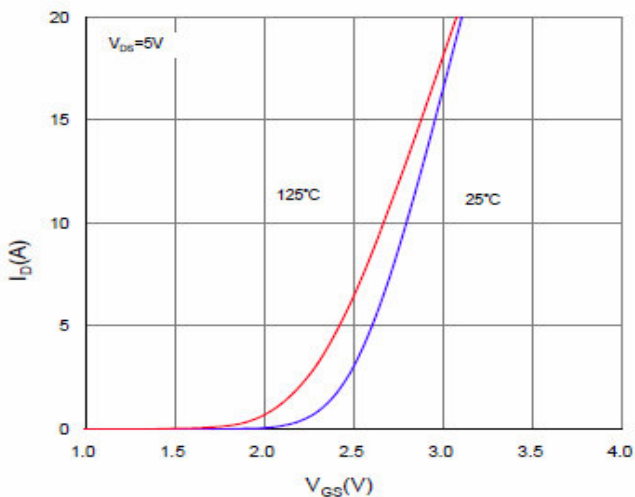


Figure 2. On-Resistance vs. Gate-Source Voltage

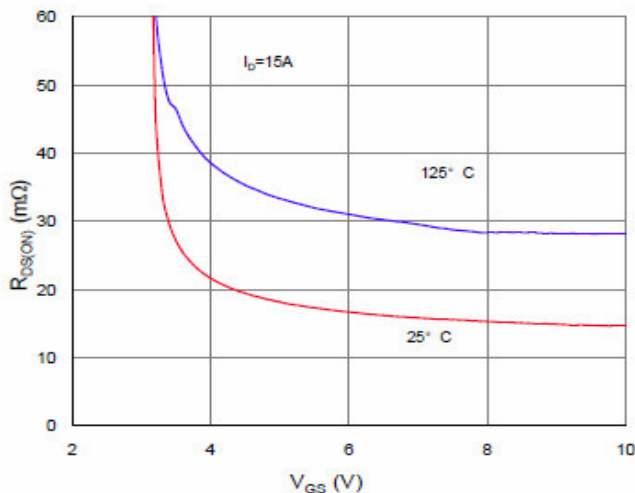


Figure 4. Normalized On-Resistance vs. Junction Temperature

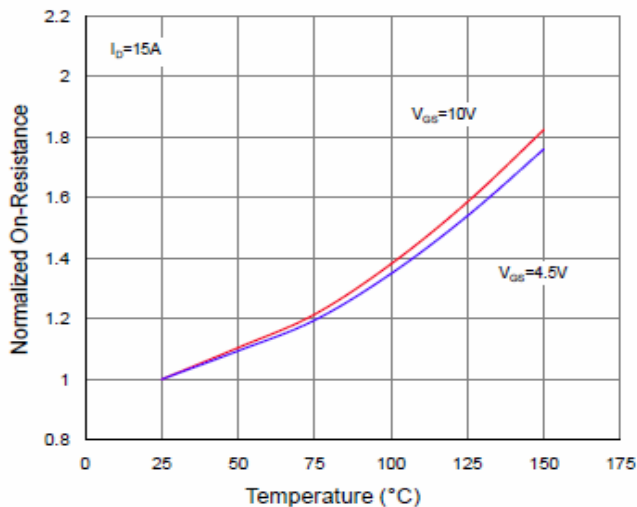
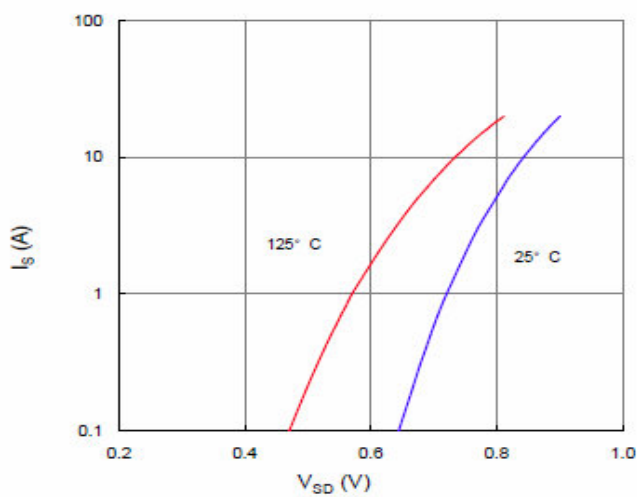


Figure 6. Typical Source-Drain Diode Forward Voltage



CHARACTERISTIC CURVES

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

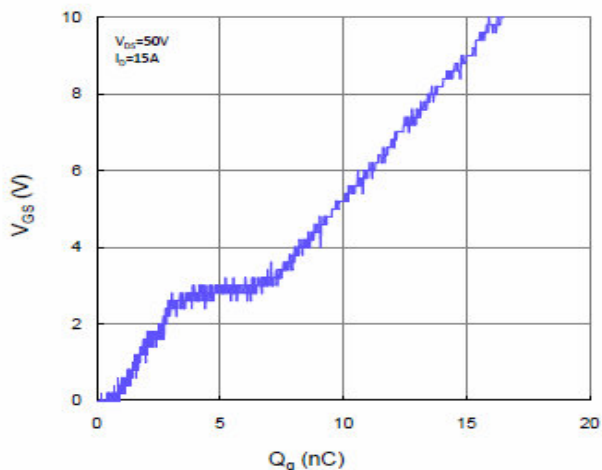


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

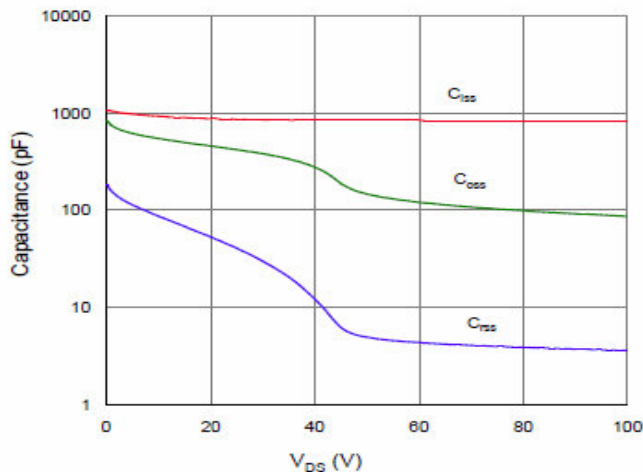


Figure 9. Maximum Safe Operating Area

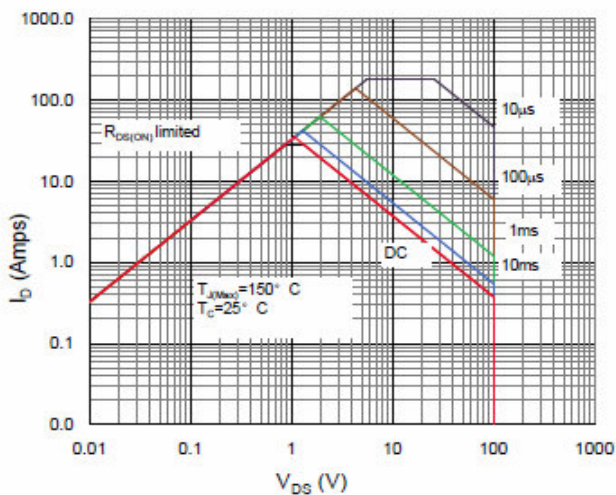


Figure 10. Maximum Drain Current vs. Case Temperature

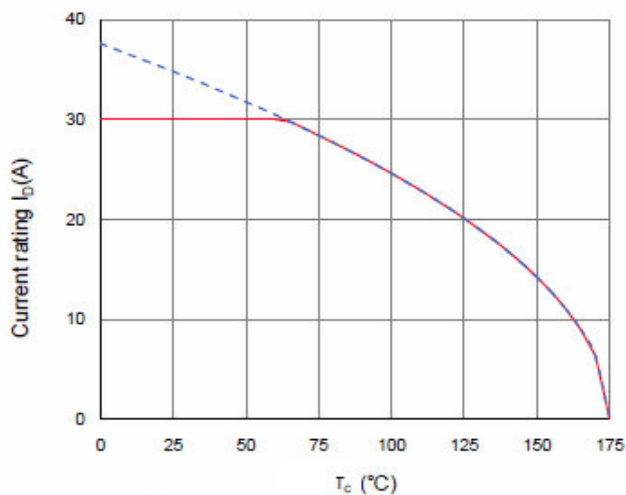


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

