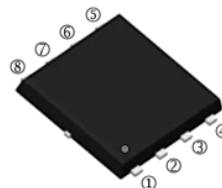


RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

These N-Channel enhancement mode power field effect transistors are using SGT MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

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FEATURES

- Fast Switching
- Improved dv/dt Capability
- Green Device Available

APPLICATIONS

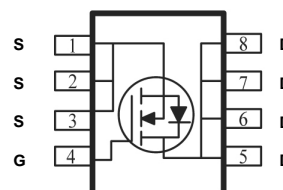
- Power Management Switches
- DC/DC Converter

PACKAGE INFORMATION

Package	MPQ	Leader Size
PR-8PP	3K	13 inch

ORDER INFORMATION

Part Number	Type
SPR90N12SV-C	Lead (Pb)-free and Halogen-free



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	120	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	90	A
Pulsed Drain Current ¹	I_{DM}	360	A
Power Dissipation	P_D	104	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Ratings			
Maximum Thermal Resistance Junction-Ambient	$R_{\theta JA}$	56	$^\circ\text{C/W}$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	1.2	

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	120	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$
Gate Threshold Voltage	$V_{GS(th)}$	2	-	4	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{V}, V_{DS}=0$
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	$V_{DS}=120\text{V}, V_{GS}=0$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	-	7.5	m Ω	$V_{GS}=10\text{V}, I_D=20\text{A}$
Gate Resistance	R_g	-	2.6	-	Ω	$V_{GS}=V_{DS}=0\text{V}, f=1\text{MHz}$
Forward Transconductance	g_{fs}	-	70	-	S	$V_{DS}=10\text{V}, I_D=20\text{A}$
Total Gate Charge	Q_g	-	43	-	nC	$V_{DS}=60\text{V}$ $V_{GS}=10\text{V}$ $I_D=20\text{A}$
Gate-Source Charge	Q_{gs}	-	13.8	-		
Gate-Drain Change	Q_{gd}	-	8	-		
Turn-on Delay Time	$T_{d(on)}$	-	14.3	-	nS	$V_{DD}=60\text{V}$ $V_{GS}=10\text{V}$ $I_D=20\text{A}$ $R_G=3\Omega$
Rise Time	T_r	-	12	-		
Turn-off Delay Time	$T_{d(off)}$	-	33.5	-		
Fall Time	T_f	-	8.6	-		
Input Capacitance	C_{iss}	-	3370	-	pF	$V_{DS}=60\text{V}$ $V_{GS}=0$ $f=1\text{MHz}$
Output Capacitance	C_{oss}	-	471	-		
Reverse Transfer Capacitance	C_{rss}	-	11	-		
Source-Drain Diode						
Continuous Source Current	I_S	-	-	90	A	$V_G=V_D=0\text{V}$, Force Current
Diode Forward Voltage	V_{SD}	-	-	1.2	V	$V_{GS}=0, I_S=20\text{A}$
Body Diode Reverse Recovery Time	t_{rr}	-	46	-	nS	$I_F=20\text{A}, di/dt=500\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	Q_{rr}	-	278	-	nC	

Notes:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed, Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

CHARACTERISTICS CURVES

FIG. 1-Transfer Characteristics

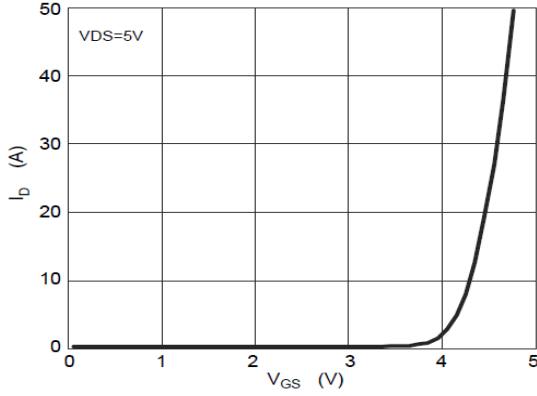


FIG. 2- I_S vs V_{SD}

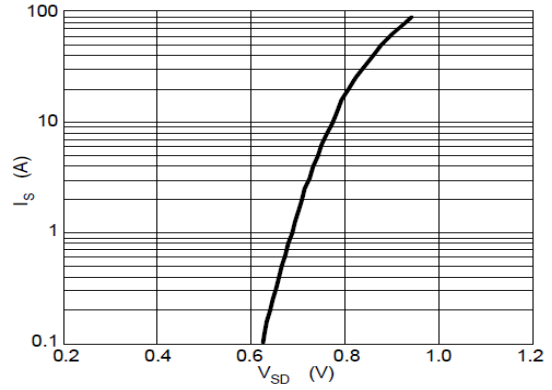


FIG. 3- $R_{DS(on)}$ vs I_D

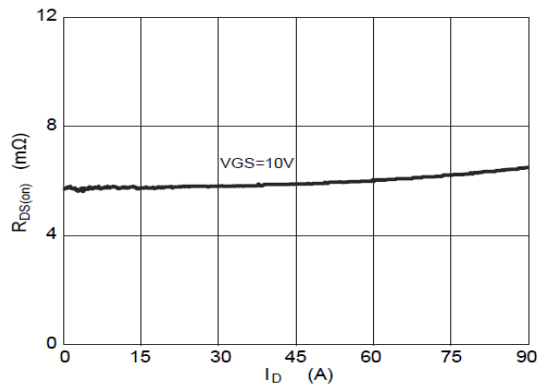


FIG. 4-Normalized $R_{DS(ON)}$ vs T_J

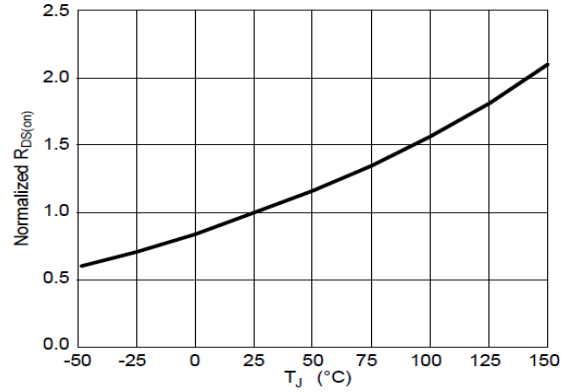


FIG. 5-Gate Charge Characteristics

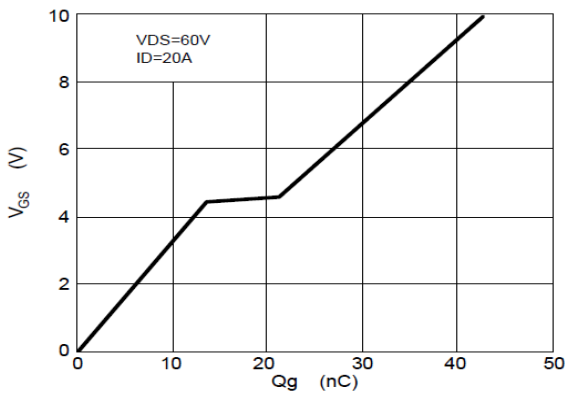


FIG. 6-Safe Operating Area

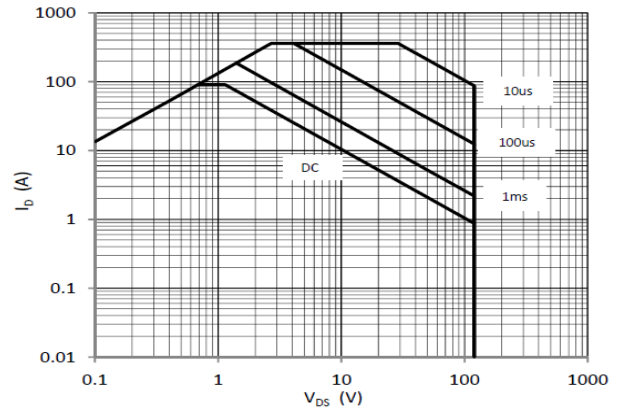
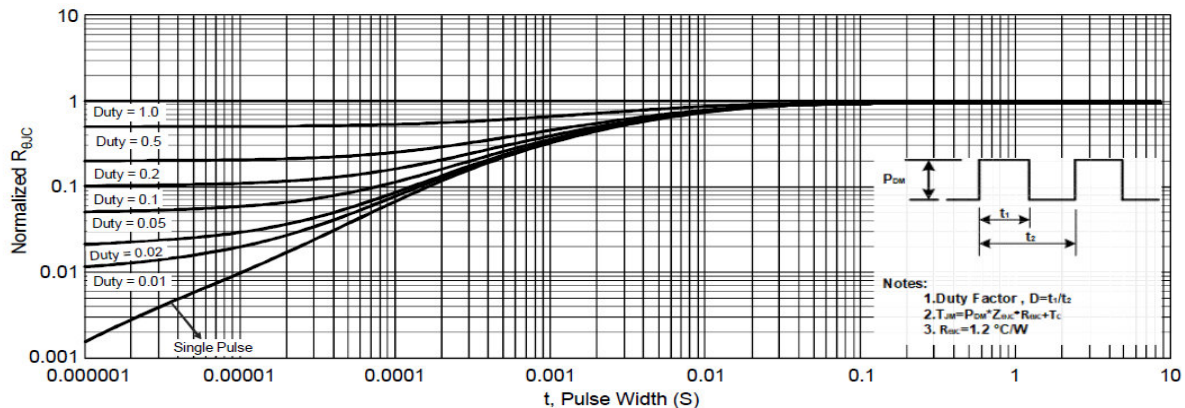
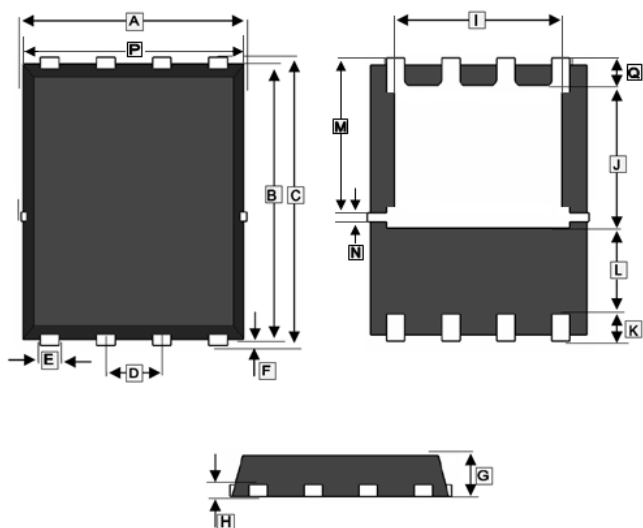


FIG. 7-Transient Thermal Impedance



PACKAGE OUTLINE DIMENSIONS

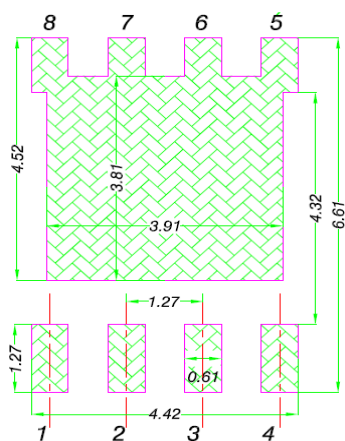
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REF.	Millimeter	
	Min.	Max.
A	4.80	5.40
B	5.45	6.06
C	5.80	6.35
D	1.27 BSC.	
E	0.30	0.51
F	0.05	0.36
G	0.80	1.30
H	0.254 REF.	
I	3.80 REF.	
J	3.60 REF.	
K	0.60 REF.	
L	1.10 REF.	
M	3.75 REF.	
N	0.25 REF.	
P	4.80	5.00
Q	0.50 REF.	

MOUNTING PAD LAYOUT

PR-8PP



*Dimensions in millimeters