

RoHS Compliant Product  
A suffix of "-C" specifies halogen & lead-free

## DESCRIPTION

The SSG4953-C is the highest performance trench Dual P-Ch MOSFETs with extreme high cell density, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the synchronous buck converter applications.

The SSG4953-C meet the RoHS and Green Product requirement with full function reliability approved.

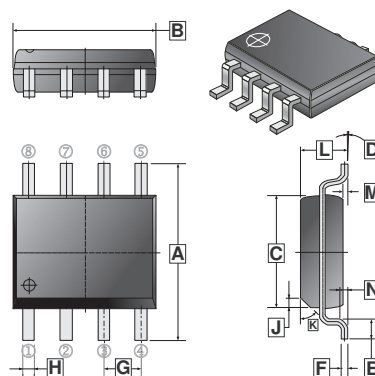
## FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

## MARKING



## SOP-8



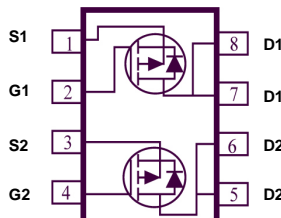
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.79	6.20	H	0.33	0.51
B	4.70	5.11	J	0.375	REF.
C	3.80	4.00	K	45°	REF.
D	0°	8°	L	1.3	1.752
E	0.40	1.27	M	0	0.25
F	0.10	0.25	N	0.25	REF.
G	1.27 TYP.				

## PACKAGE INFORMATION

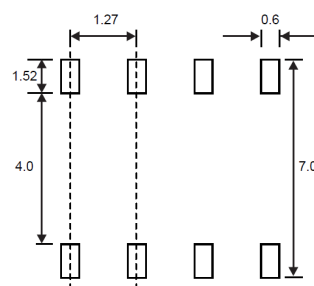
Package	MPQ	Leader Size
SOP-8	2.5K	13 inch

## ORDER INFORMATION

Part Number	Type
SSG4953-C	Lead (Pb)-free and Halogen-free



## Mounting Pad Layout



\*Dimensions in millimeters

## MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current @ $V_{GS} = -10V$ <sup>1</sup>	$I_D$	$T_A = 25^\circ C$	-4.9
		$T_A = 70^\circ C$	-3.9
Pulsed Drain Current <sup>3</sup>	$I_{DM}$	-10	A
Total Power Dissipation	$P_D$	1.5	W
Operating Junction & Storage Temperature Range	$T_J, T_{STG}$	-55~150	$^\circ C$
<b>Thermal Resistance Ratings</b>			
Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	83	$^\circ C/W$
Thermal Resistance Junction-Ambient <sup>2</sup>		125	
Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	50	

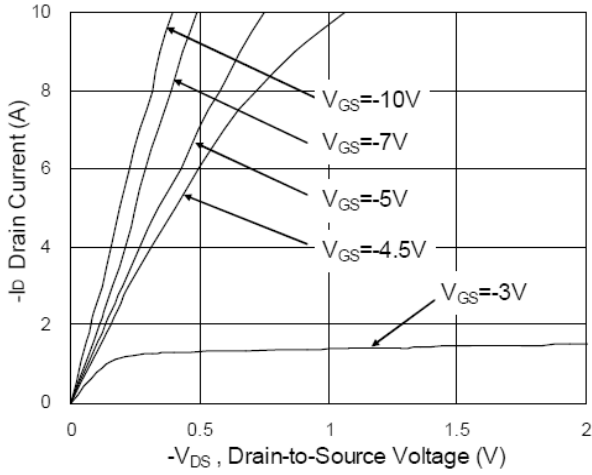
**ELECTRICAL CHARACTERISTICS** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Drain-Source Breakdown Voltage	$BV_{DSS}$	-30	-	-	V	$V_{GS}=0, I_D = -250\mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	-1	-	-2.5	V	$V_{DS}=V_{GS}, I_D = -250\mu\text{A}$	
Forward Transconductance	$g_{fs}$	-	6	-	S	$V_{DS} = -10\text{V}, I_D = -4\text{A}$	
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS} = \pm 20\text{V}$	
Drain-Source Leakage Current	$I_{DSS}$	$T_J=25^\circ\text{C}$	-	-	-1	$\mu\text{A}$	$V_{DS} = -24\text{V}, V_{GS}=0$
		$T_J=55^\circ\text{C}$	-	-	-5		$V_{DS} = -24\text{V}, V_{GS}=0$
Static Drain-Source On-Resistance <sup>4</sup>	$R_{DS(ON)}$	-	-	48	m $\Omega$	$V_{GS} = -10\text{V}, I_D = -4\text{A}$	
		-	-	82		$V_{GS} = -4.5\text{V}, I_D = -3\text{A}$	
Total Gate Charge	$Q_g$	-	6.4	-	nC	$I_D = -4\text{A}$ $V_{DS} = -20\text{V}$ $V_{GS} = -4.5\text{V}$	
Gate-Source Charge	$Q_{gs}$	-	2.2	-			
Gate-Drain Charge	$Q_{gd}$	-	2.3	-			
Turn-on Delay Time	$T_{d(on)}$	-	9	-	nS	$V_{DS} = -12\text{V}$ $I_D = -4\text{A}$ $V_{GS} = -10\text{V}$ $R_G = 3.3\Omega$	
Rise Time	$T_r$	-	16.6	-			
Turn-off Delay Time	$T_{d(off)}$	-	21	-			
Fall Time	$T_f$	-	21.6	-			
Input Capacitance	$C_{iss}$	-	632	-	pF	$V_{GS}=0$ $V_{DS} = -15\text{V}$ $f=1\text{MHz}$	
Output Capacitance	$C_{oss}$	-	100	-			
Reverse Transfer Capacitance	$C_{rss}$	-	74	-			
<b>Source-Drain Diode</b>							
Continuous Source Current <sup>1</sup>	$I_S$	-	-	-4.9	A		
Pulsed Source Current <sup>3</sup>	$I_{SM}$	-	-	-10			
Forward on Voltage <sup>4</sup>	$V_{SD}$	-	-	-1.2	V	$I_S = -1\text{A}, V_{GS}=0$	

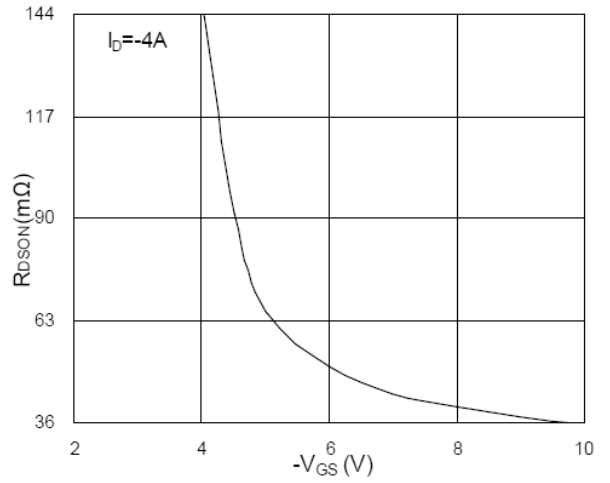
Notes:

- Surface Mounted on 1"x1" FR-4 Board with 2oz copper.
- When mounted on Min. copper pad.
- Pulse width limited by maximum junction temperature, Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

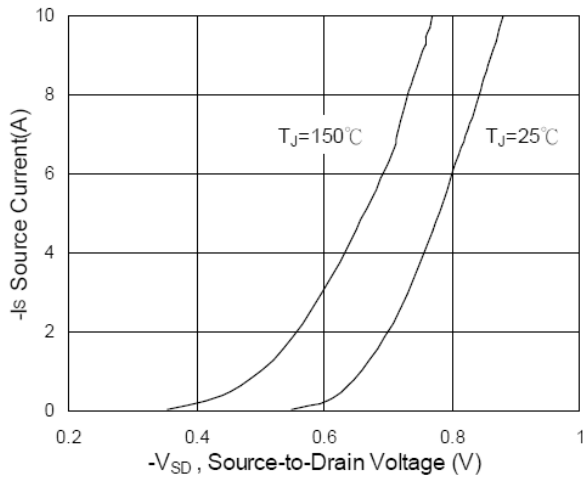
**CHARACTERISTIC CURVES**



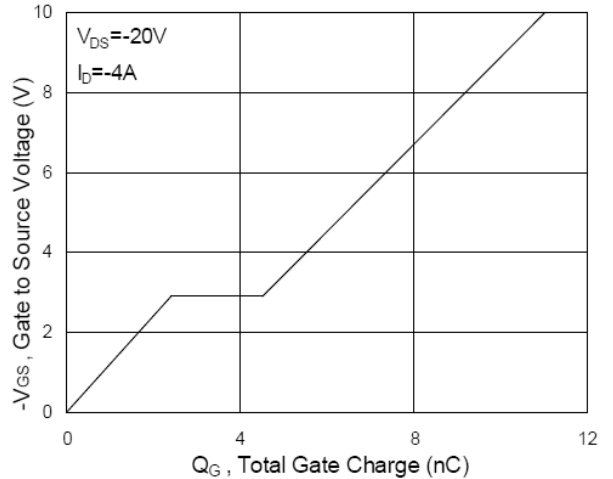
**Fig.1 Typical Output Characteristics**



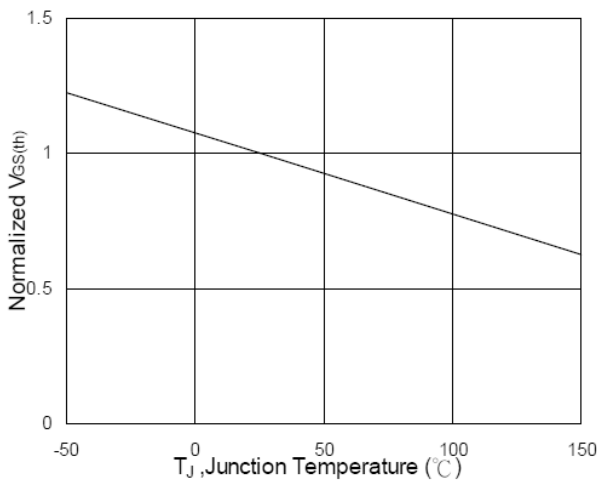
**Fig.2 On-Resistance vs. Gate-Source**



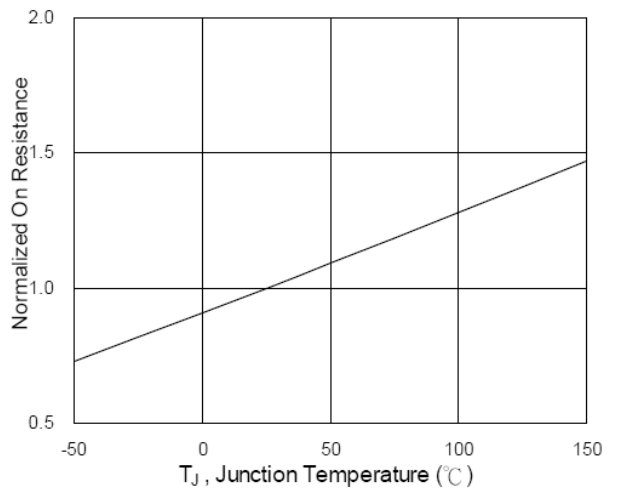
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

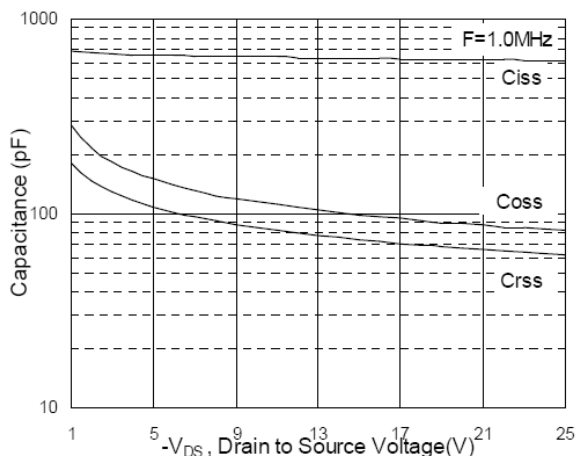


**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**

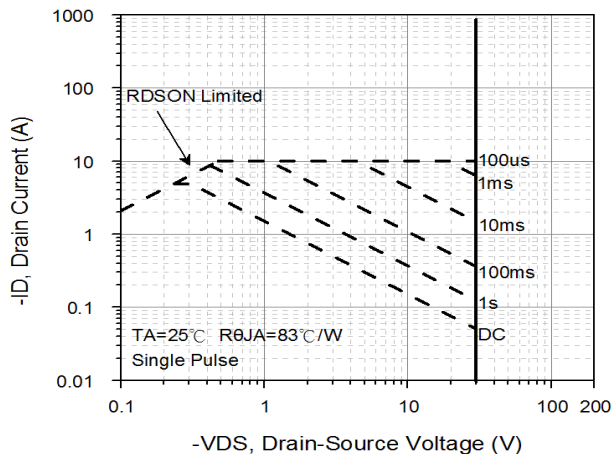


**Fig.6 Normalized  $R_{DS(ON)}$  vs.  $T_J$**

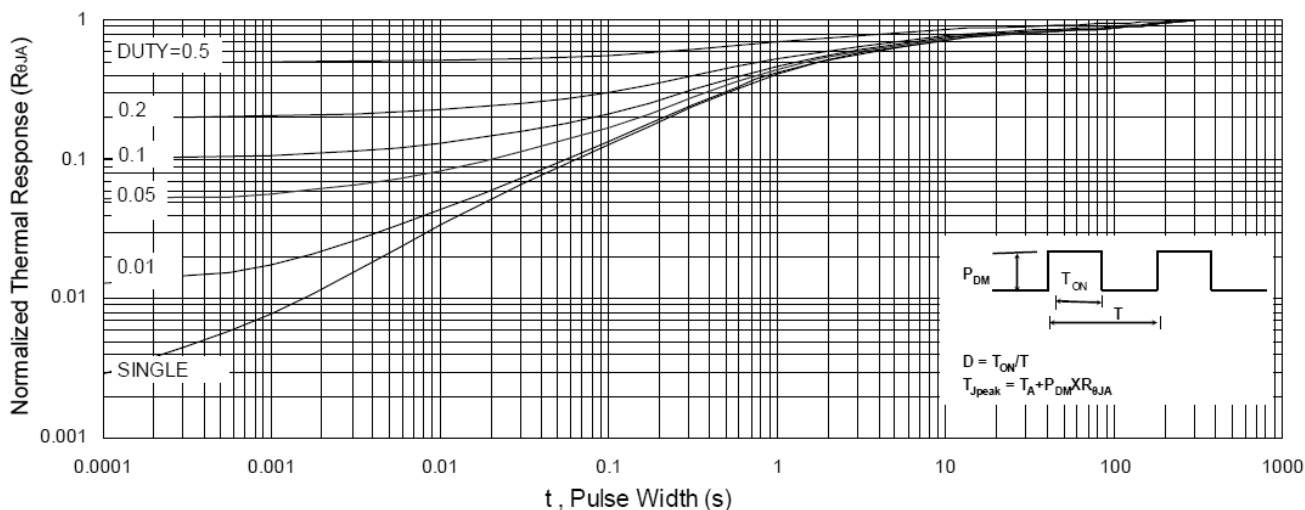
**CHARACTERISTIC CURVES**



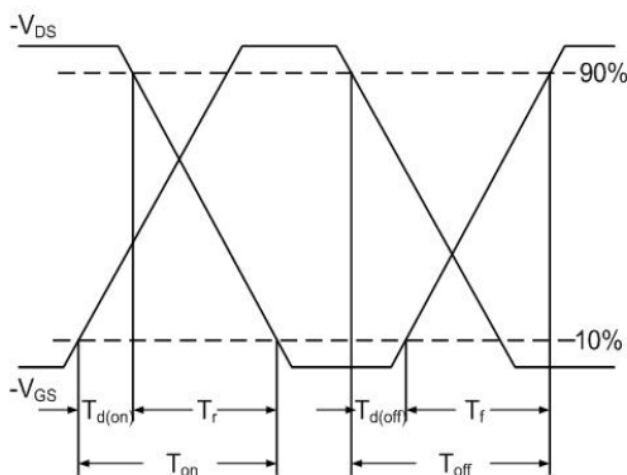
**Fig.7 Capacitance**



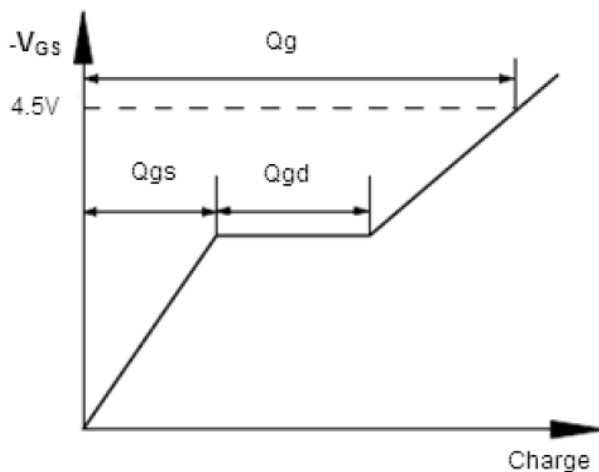
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**