SSP45N10

45A , 100V , $R_{DS(ON)}$ 22 mΩ
N-Channel Enhancement Mode MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

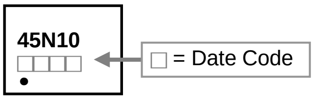
DESCRIPTION

The SSP45N10 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications .The SSP45N10 meet the RoHS and Green Product requirement , 100% EAS guaranteed with full function reliability approved.

FEATURES

- Simple Drive Requirement
- Small Package Outline

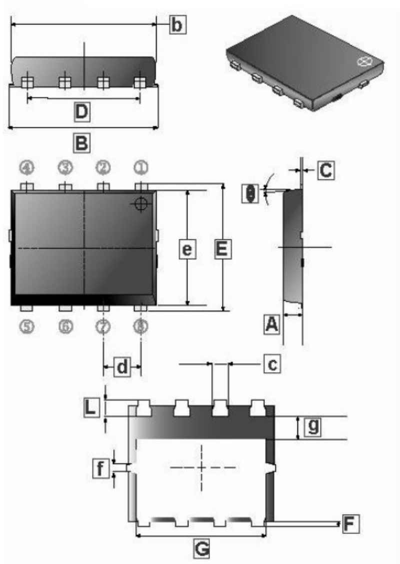
MARKING



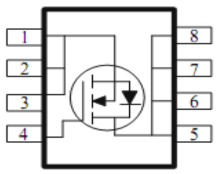
PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8PP	3K	13 inch

SOP-8PP



TOP VIEW



REF.	Millimeter Min.	Millimeter Max.	REF.	Millimeter Min.	Millimeter Max.
A	0.80	1.00	θ	0°	10°
B	5.3 BSC.		b	5.2 BCS	
C	0.15	0.25	c	0.20	0.50
D	3.8 BCS.		d	1.27BSC	
E	6.05 BCS.		e	5.65 BCS.	
F	0.03	0.30	f	0.10	0.40
G	4.35 BCS.		g	1.3 BCS.	
L	0.40	0.70			

ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1] , V_{GS}@10V	T_C=25℃	I_D	45	A
	T_C=100℃		28	
Pulsed Drain Current [2]	T_C=25℃	I_{DM}	100	A
Power Dissipation [4]	T_C=25℃	P_D	90	W
Single Pulse Avalanche Energy [3]		E_{AS}	98	mJ
Single Pulse Avalanche Current		I_{AS}	41	A
Operating Junction and Storage Temperature Range		T_j, T_{stg}	-55~150	℃
Thermal Resistance Rating				
Maximum Junction to Case [1]		$R_{θJC}$	1.4	℃ / W
Maximum Junction to Ambient [1]		$R_{θJA}$	36	℃ / W

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static							
Drain-Source Breakdown Voltage		BV_{DSS}	100	-	-	V	V_{GS}=0, I_D=250μA
Gate-Threshold Voltage		$V_{GS(th)}$	2	-	4	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transconductance		g_{fs}	-	27	-	S	V_{DS}=5V, I_D=30A
Gate Resistance		R_G	-	1.9	3.8	Ω	f=1MHz
Gate-Body Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}=±20V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	1	μA	V_{DS}=80V, V_{GS}=0
	T_J=55℃		-	-	5		V_{DS}=80V, V_{GS}=0
Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	19	22	mΩ	V_{GS}=10V, I_D=30A
			-	25	30		V_{GS}=7V, I_D=15A
Dynamic							
Total Gate Charge		Q_g	-	27.6	-	nC	V_{DS}=80V, V_{GS}=10V, I_D=30A
Gate-Source Charge		Q_{gs}	-	11.4	-		
Gate-Drain (“Miller”) Charge		Q_{gd}	-	7.9	-		
Turn-on Delay Time[2]		$T_{d(on)}$	-	15.6	-	nS	V_{DD}=50V, V_{GS}=10V, R_G=3.3Ω, I_D=30A
Rise Time		T_r	-	17.2	-		
Turn-off Delay Time		$T_{d(off)}$	-	16.8	-		
Fall Time		T_f	-	9.2	-		
Input Capacitance		C_{iss}	-	1890	-	pF	V_{GS}=0, V_{DS}=15V, f=1.0MHz
Output Capacitance		C_{oss}	-	268	-		
Reverse Transfer Capacitance		C_{rss}	-	67	-		
Guaranteed Avalanche Chatacteristics							
Single Pulse Avalanche Energy[5]		EAS	53	-	-	mJ	V_{DD}=50V,L=0.1mH, I_{AS} =30A
Source-Drain Diode							
Diode Forward Voltage[2]		V_{SD}	-	-	1	V	I_S=1A, V_{GS}=0
Continuous Source Current [1,6]		I_S	-	-	45	A	V_D=V_G=0, Force Current
Pulsed Source Current [2,6]		I_{SM}	-	-	100	A	
Reverse Recovery Time		T_{RR}	-	34	-	ns	I_F=30A, T_J=25℃ dI/dt=100A/μs
Reverse Recovery Charge		Q_{RR}	-	47	-	nC	

Notes:
1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper , ≦10sec , 125℃/W at steady state
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3. The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=53.8A
4. The power dissipation is limited by 150℃ junction temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation

CHARACTERISTIC CURVES

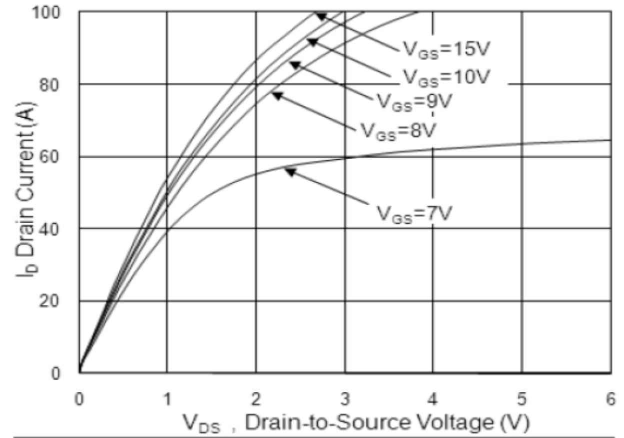


Fig.1 Typical Output Characteristics

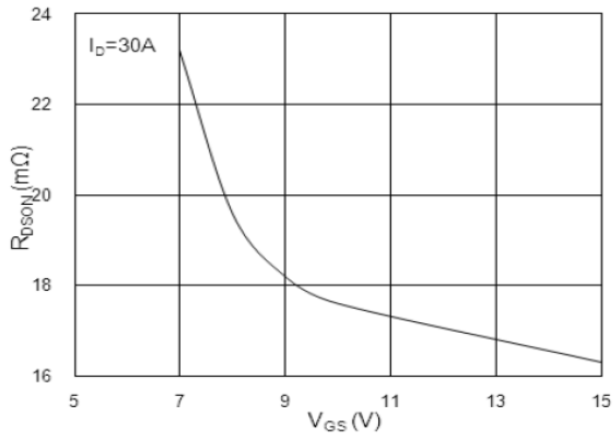


Fig.2 On-Resistance v.s Gate-Source

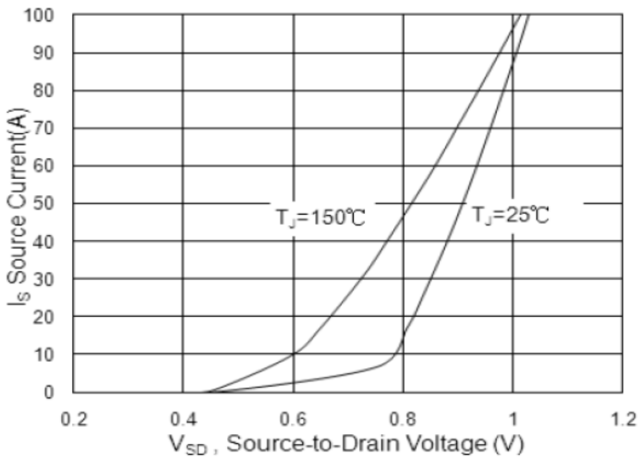


Fig.3 Forward Characteristics of Reverse

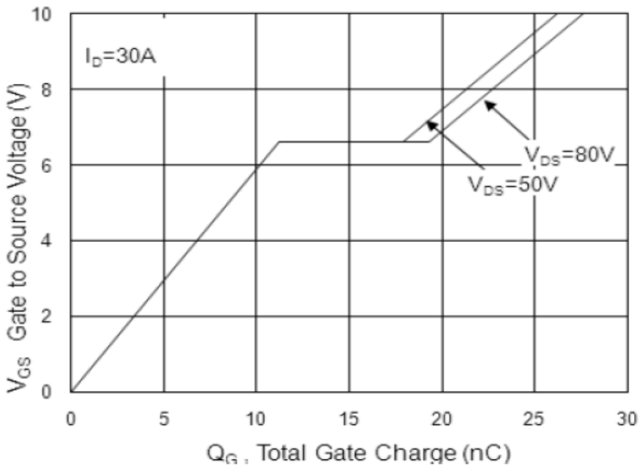


Fig.4 Gate-Charge Characteristics

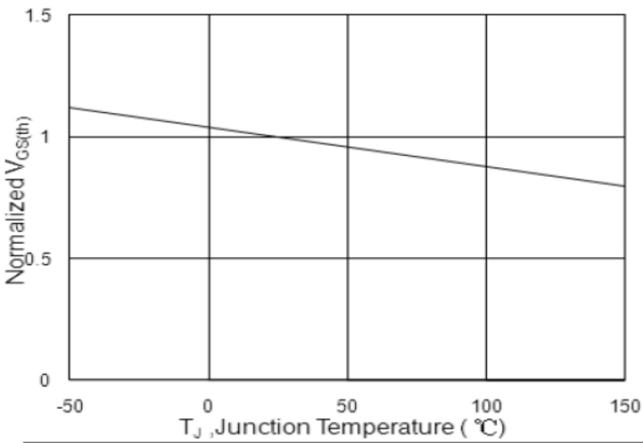


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

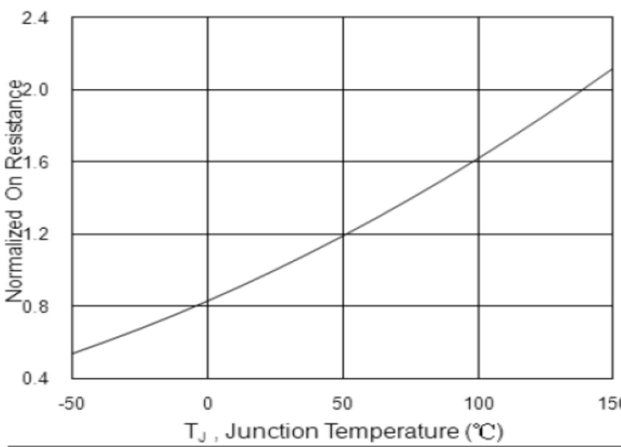


Fig.6 Normalized R_{DSON} v.s T_J

CHARACTERISTIC CURVES

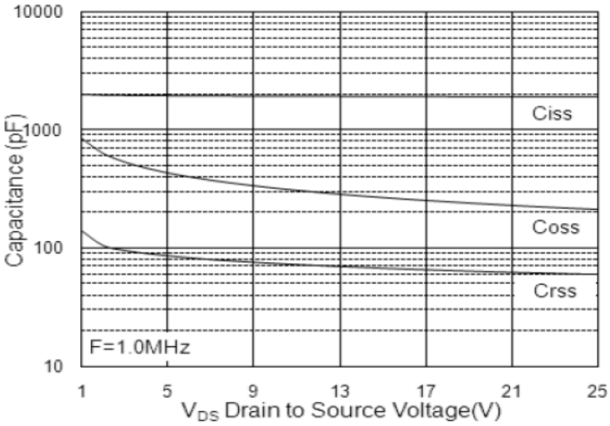


Fig.7 Capacitance

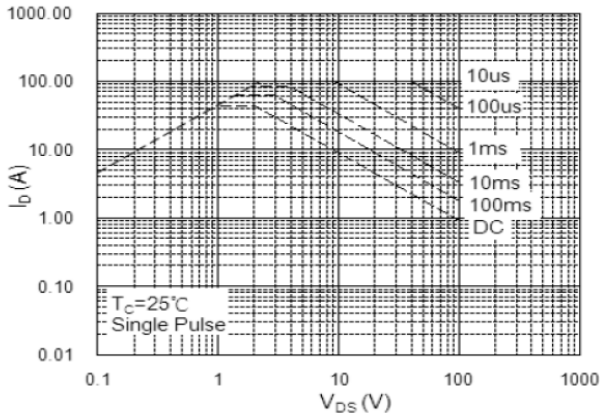


Fig.8 Safe Operating Area

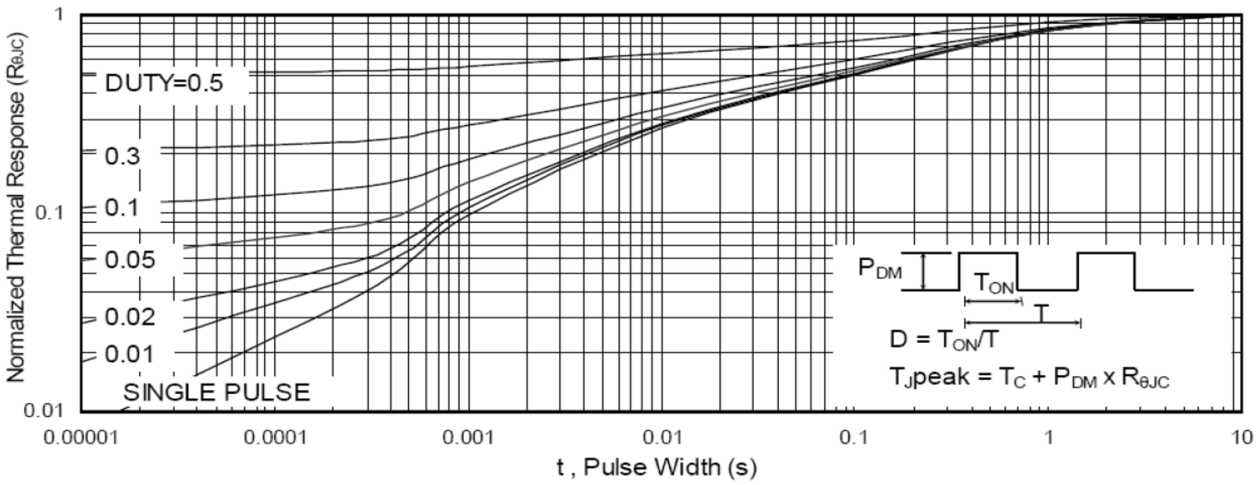


Fig.9 Normalized Maximum Transient Thermal Impedance

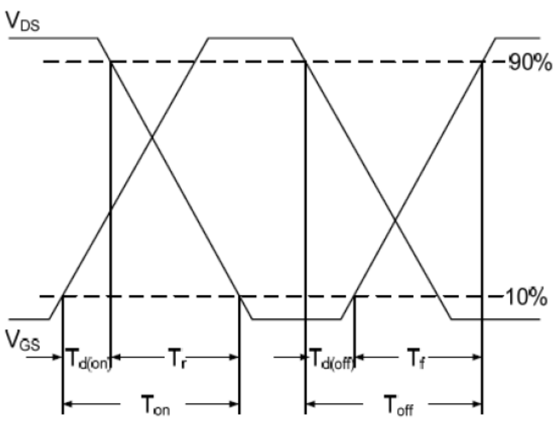


Fig.10 Switching Time Waveform

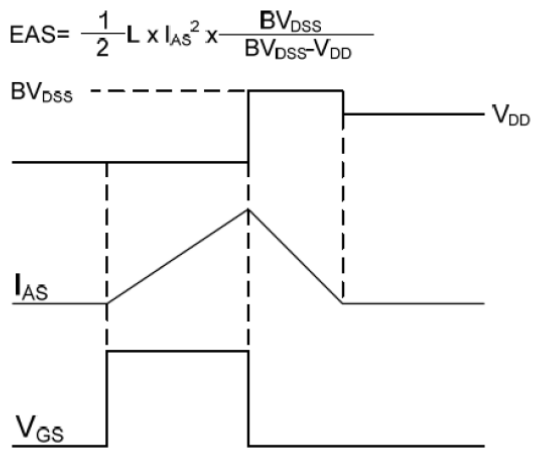


Fig.11 Unclamped Inductive Switching Waveform