

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

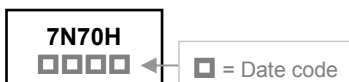
The SSM1K7N70H-C is power MOSFET using Super Junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of low EMI to designers as well as low switching loss, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSM1K7N70H-C meet the RoHS and Green Product requirement with full function reliability approved.

FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING



PACKAGE INFORMATION

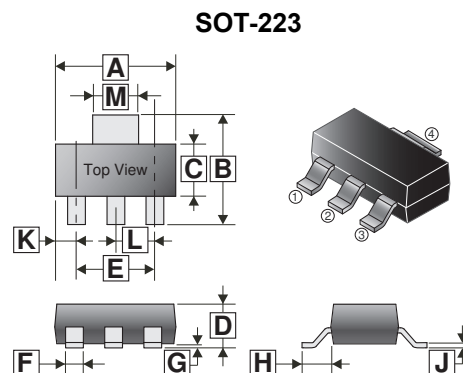
Package	MPQ	Leader Size
SOT-223	2.5K	13 inch

ORDER INFORMATION

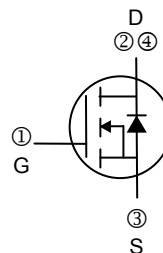
Part Number	Type
SSM1K7N70H-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	
Drain-Source Voltage	V_{DS}	700	V	
Gate-Source Voltage	V_{GS}	± 30	V	
Continuous Drain Current ¹ @ $V_{GS}=10V$	$T_A=25^\circ C$	1	A	
	$T_A=70^\circ C$	0.8		
Pulsed Drain Current ³	I_{DM}	4	A	
Total Power Dissipation ¹	$T_A=25^\circ C$	P_D	2.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ C$	
Thermal Resistance Rating				
Thermal Resistance from Junction-Ambient ¹	$R_{\theta JA}$	$t \leq 10\text{sec}, 50$	$^\circ C / W$	
		Steady State, 100		
Thermal Resistance from Junction-Ambient ²		125		
Thermal Resistance from Junction-Case	$R_{\theta JC}$	30		



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.90	6.70	G	-	0.18
B	6.70	7.30	H	2.00 REF.	
C	3.30	3.80	J	0.20	0.40
D	1.40	1.90	K	1.10 REF.	
E	4.45	4.75	L	2.30 REF.	
F	0.60	0.85	M	2.80	3.20



ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	BV_{DSS}	700	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$
Gate Threshold Voltage	$V_{GS(th)}$	2	-	4	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 30\text{V}$
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	$V_{DS}=560\text{V}, V_{GS}=0$
Static Drain-Source On-Resistance ⁴	$R_{DS(ON)}$	-	1.5	1.7	Ω	$V_{GS}=10\text{V}, I_D=1\text{A}$
Total Gate Charge	Q_g	-	6.1	-	nC	$I_D=1\text{A}$ $V_{DS}=560\text{V}$ $V_{GS}=10\text{V}$
Gate-Source Charge	Q_{gs}	-	1.3	-		
Gate-Drain ("Miller") Charge	Q_{gd}	-	3.3	-		
Turn-On Delay Time	$T_{d(on)}$	-	11	-	nS	$V_{DS}=350\text{V}$ $I_D=1\text{A}$ $V_{GS}=10\text{V}$ $R_G=25\Omega$
Rise Time	T_r	-	25	-		
Turn-Off Delay Time	$T_{d(off)}$	-	30	-		
Fall Time	T_f	-	24	-		
Input Capacitance	C_{iss}	-	225	-	pF	$V_{GS}=0\text{V}$ $V_{DS}=25\text{V}$ $f=1\text{MHz}$
Output Capacitance	C_{oss}	-	300	-		
Reverse Transfer Capacitance	C_{rss}	-	12	-		
Source-Drain Diode						
Continuous Source Current ¹	I_S	-	-	1	A	
Pulsed Source Current ³	I_{SM}	-	-	4	A	
Forward On Voltage ⁴	V_{SD}	-	-	1.4	V	$I_S=1\text{A}, V_{GS}=0\text{V}$
Reverse Recovery Time	T_{rr}	-	358	-	nS	$I_F=1\text{A}, dI/dt=100\text{A}/\mu\text{s}$,
Reverse Recovery Charge	Q_{rr}	-	1.5	-	nC	$V_{DD}=100\text{V}, T_J=25^\circ\text{C}$

Notes:

- Surface mounted on a 1 inch² FR-4 board with 20Z copper.
- When mounted on Min. copper pad.
- Pulse width limited by maximum junction temperature. Pulse width $\leq 10\mu\text{s}$, Duty cycle $\leq 2\%$.
- Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTIC CURVES

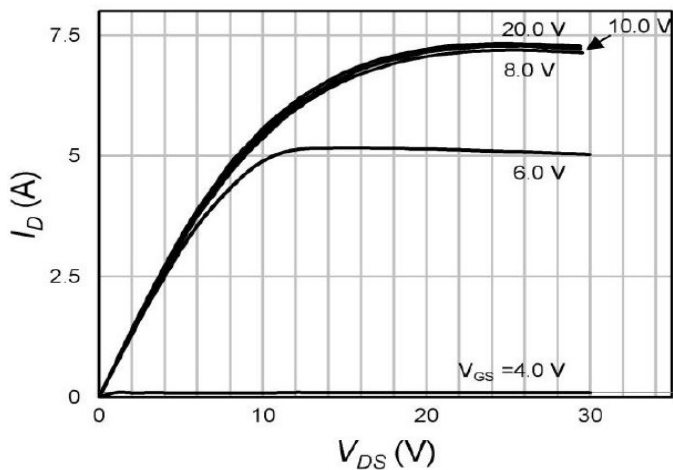


Fig.1 Typical Output Characteristics

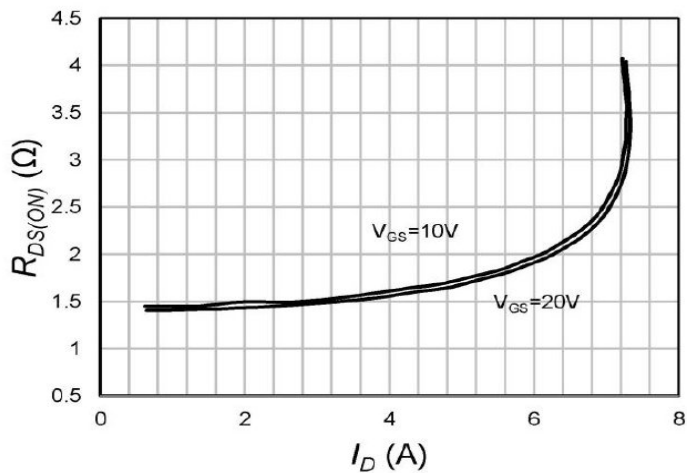


Fig.2 On-Resistance vs. Drain Current

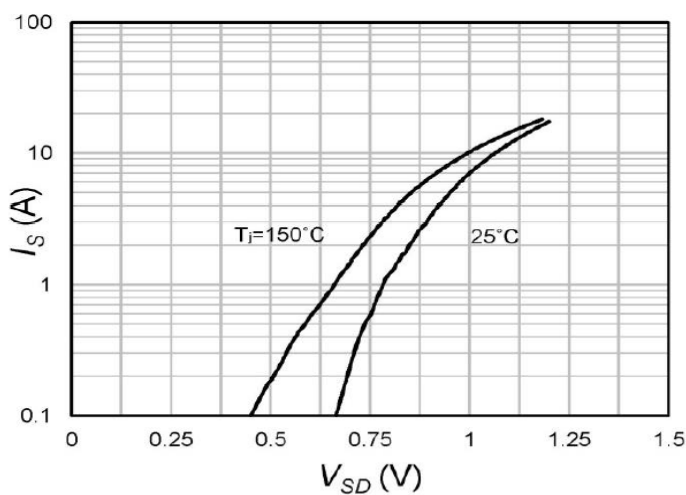


Fig.3 Forward Characteristics of Reverse

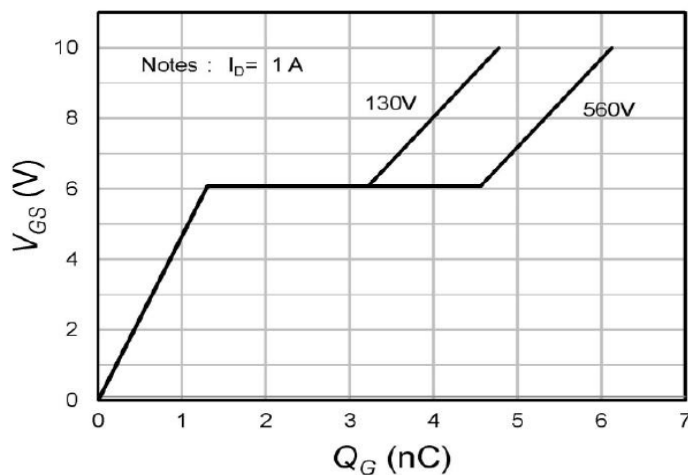


Fig.4 Gate-Charge Characteristics

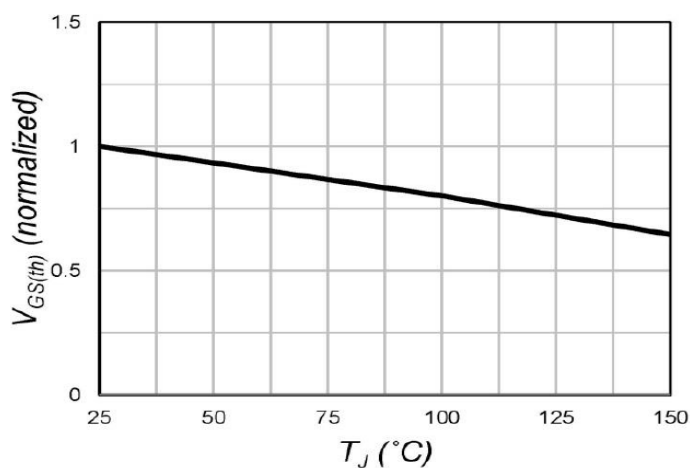


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

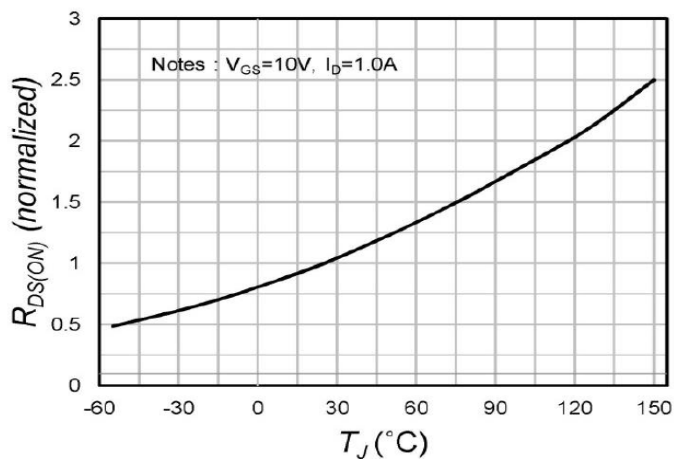


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

TYPICAL CHARACTERISTIC CURVES

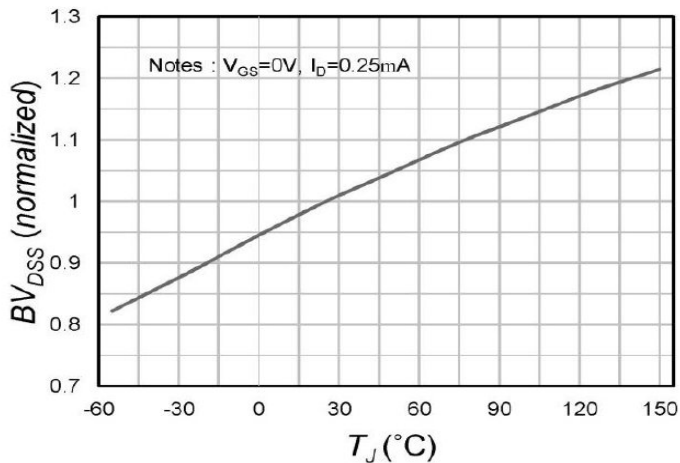


Fig.7 Drain-Source Breakdown Voltage(Normazied)

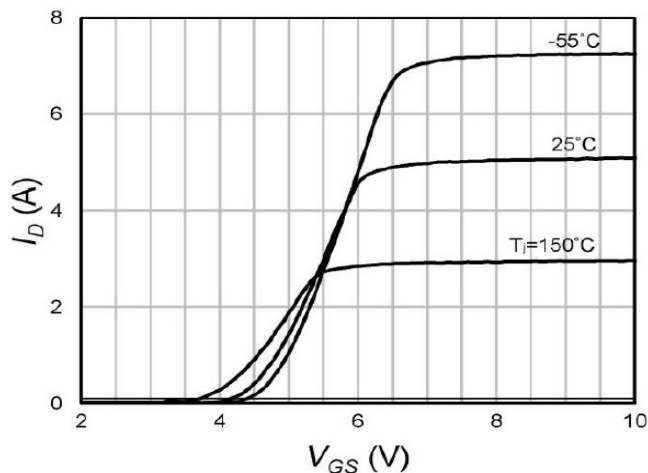


Fig.8 Transfer Characteristics

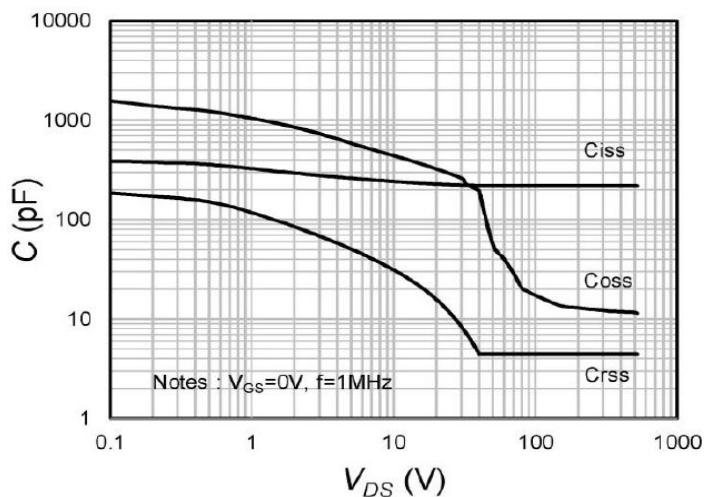


Fig.9 Capacitances

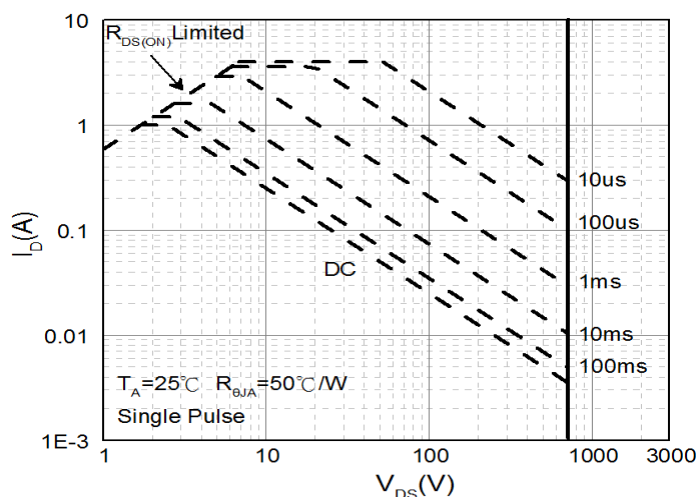


Fig.10 Safe Operating Area

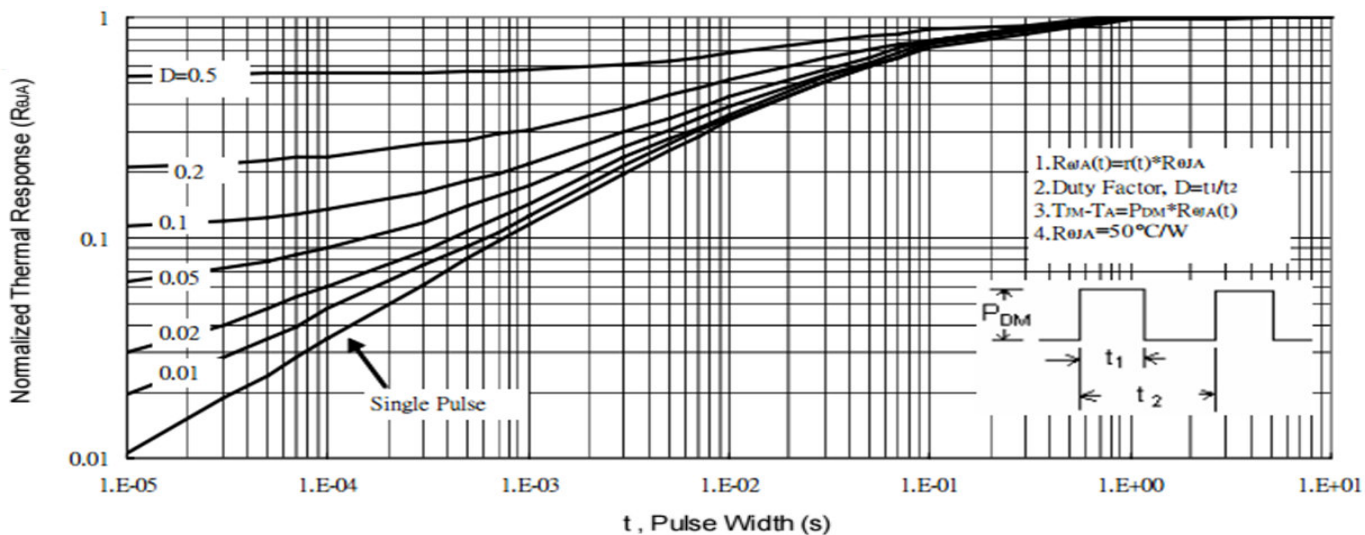


Fig.11 Normalized Maximum Transient Thermal Impedance