Elektronische Bauelemente

# SST3585S-C

**4.3A, 20V, $R_{DS(ON)}$ 37mΩ**
**-3.1A, -20V, $R_{DS(ON)}$ 75mΩ**
**N & P-Ch Enhancement Mode Power MOSFET**

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

## DESCRIPTION

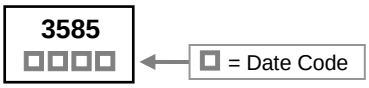
The SST3585S-C is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The SST3585S-C meet the RoHS and Green Product requirement with full function reliability approved.

## FEATURES

- Low Gate Charge
- Low On-resistance

## MARKING



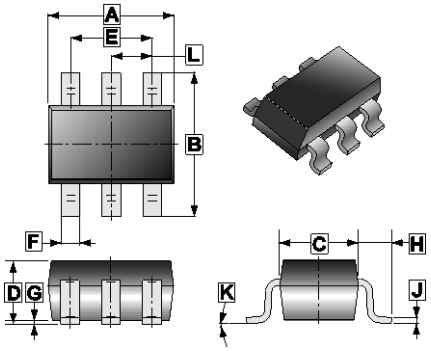

## PACKAGE INFORMATION

| Package | MPQ | Leader Size |
|---|---|---|
| SOT-26 | 3K | 7 inch |

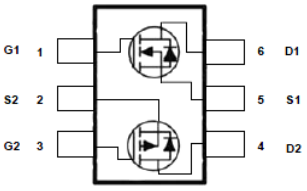
## ORDER INFORMATION

| Part Number | Type |
|---|---|
| SST3585S-C | Lead (Pb)-free and Halogen-free |

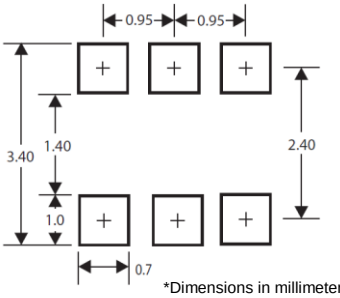
**SOT-26**




| REF. | Millimeter | | REF. | Millimeter | |
|---|---|---|---|---|---|
| | Min. | Max. | | Min. | Max. |
| A | 2.70 | 3.10 | G | 0 | 0.10 |
| B | 2.60 | 3.00 | H | 0.60 REF. | |
| C | 1.40 | 1.80 | J | 0.12 REF. | |
| D | - | 1.30 | K | 0° | 10° |
| E | 1.90 REF. | | L | 0.95 REF. | |
| F | 0.25 | 0.50 | | | |




**Mounting Pad Layout**




*Dimensions in millimeters

## ABSOLUTE MAXIMUM RATINGS ($T_A$=25°C unless otherwise specified)

| Parameter | | Symbol | Rating | | Unit |
|---|---|---|---|---|---|
| | | | N-Ch | P-Ch | |
| Drain-Source Voltage | | $V_{DS}$ | 20 | -20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±12 | ±12 | V |
| Continuous Drain Current [1] @$V_{GS}$=4.5V | $T_A$=25°C | $I_D$ | 4.3 | -3.1 | A |
| | $T_A$=70°C | | 3.4 | -2.5 | |
| Pulsed Drain Current [3] | | $I_{DM}$ | 17.2 | -12.4 | A |
| Power Dissipation | | $P_D$ | 1.14 | | W |
| Operating Junction & Storage Temperature Range | | $T_J$, $T_{STG}$ | -55~150 | | °C |
| **Thermal Date** | | | | | |
| Maximum Thermal Resistance from Junction-Ambient [1] | | $R_{\theta JA}$ | 110 | | °C/W |
| Maximum Thermal Resistance from Junction-Ambient [2] | | | 180 | | |

## N-CH ELECTRICAL CHARACTERISTICS ($T_J$=25°C unless otherwise specified)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | | $BV_{DSS}$ | 20 | - | - | V | $V_{GS}$=0, $I_D$=250μA |
| Gate Threshold Voltage | | $V_{GS(th)}$ | 0.5 | - | 1.2 | V | $V_{DS}$=$V_{GS}$, $I_D$=250μA |
| Forward Transfer Conductance | | $g_{fs}$ | - | 20 | - | S | $V_{DS}$=5V, $I_D$=4A |
| Gate-Source Leakage Current | | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$= ±12V |
| Drain-Source Leakage Current | $T_J$=25°C | $I_{DSS}$ | - | - | 1 | μA | $V_{DS}$=16V, $V_{GS}$=0 |
| | $T_J$=55°C | | - | - | 5 | | |
| Static Drain-Source On-Resistance [4] | | $R_{DS(ON)}$ | - | - | 37 | mΩ | $V_{GS}$=4.5V, $I_D$=4A |
| | | | - | - | 45 | | $V_{GS}$=2.5V, $I_D$=3A |
| Total Gate Charge | | $Q_g$ | - | 8.6 | - | nC | $I_D$=4A<br>$V_{DS}$=15V<br>$V_{GS}$=4.5V |
| Gate-Source Charge | | $Q_{gs}$ | - | 1.37 | - | | |
| Gate-Drain Change | | $Q_{gd}$ | - | 2.3 | - | | |
| Turn-on Delay Time | | $T_{d(on)}$ | - | 5.2 | - | nS | $V_{DS}$=10V<br>$V_{GS}$=4.5V<br>$I_D$=4A<br>$R_G$=3.3Ω<br>$R_D$=2.5Ω |
| Rise Time | | $T_r$ | - | 34 | - | | |
| Turn-off Delay Time | | $T_{d(off)}$ | - | 23 | - | | |
| Fall Time | | $T_f$ | - | 9.2 | - | | |
| Input Capacitance | | $C_{iss}$ | - | 635 | - | pF | $V_{GS}$=0<br>$V_{DS}$=15V<br>f=1MHz |
| Output Capacitance | | $C_{oss}$ | - | 70 | - | | |
| Reverse Transfer Capacitance | | $C_{rss}$ | - | 63 | - | | |
| **Source-Drain Diode** | | | | | | | |
| Forward on Voltage [4] | | $V_{SD}$ | - | 0.7 | 1.2 | V | $I_S$=1A, $V_{GS}$=0 |
| Continuous Source Current [1] | | $I_S$ | - | - | 4.3 | A | |
| Pulsed Source Current [3] | | $I_{SM}$ | - | - | 17.2 | | |
| Reverse Recovery Time | | $T_{rr}$ | - | 7.5 | - | nS | $I_S$=4A, $V_{GS}$=0<br>dI/dt=100A/μs |
| Reverse Recovery Charge | | $Q_{rr}$ | - | 2.1 | - | nC | |

Notes:
1. Surface mounted on a 1 inch$^2$ FR-4 board with 2oz copper. t≦5s.
2. Surface mounted on FR-4 Board using the minimum recommended pad size.
3. The power dissipation is limited by 150°C junction temperature, Pw≤300μs, Duty cycle≤1%.
4. The data tested by pulsed, pulse width≤300μs, duty cycle≤2%.

## P-CH ELECTRICAL CHARACTERISTICS ($T_J$=25°C unless otherwise specified)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | | $BV_{DSS}$ | -20 | - | - | V | $V_{GS}$=0, $I_D$= -250μA |
| Gate Threshold Voltage | | $V_{GS(th)}$ | -0.5 | - | -1.2 | V | $V_{DS}$=$V_{GS}$, $I_D$= -250μA |
| Forward Transfer Conductance | | $g_{fs}$ | - | 9 | - | S | $V_{DS}$= -5V, $I_D$= -3A |
| Gate-Source Leakage Current | | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$= ±12V |
| Drain-Source Leakage Current | $T_J$=25°C | $I_{DSS}$ | - | - | -1 | μA | $V_{DS}$= -16V, $V_{GS}$=0 |
| | $T_J$=55°C | | - | - | -5 | | |
| Static Drain-Source On-Resistance [4] | | $R_{DS(ON)}$ | - | - | 75 | mΩ | $V_{GS}$= -4.5V, $I_D$= -3A |
| | | | - | - | 105 | | $V_{GS}$= -2.5V, $I_D$= -2A |
| Total Gate Charge | | $Q_g$ | - | 9.7 | - | nC | $I_D$= -3A<br>$V_{DS}$= -15V<br>$V_{GS}$= -4.5V |
| Gate-Source Charge | | $Q_{gs}$ | - | 2.05 | - | | |
| Gate-Drain Change | | $Q_{gd}$ | - | 2.43 | - | | |
| Turn-on Delay Time | | $T_{d(on)}$ | - | 4.8 | - | nS | $V_{DS}$= -10V<br>$V_{GS}$= -4.5V<br>$I_D$= -3A<br>$R_G$=3.3Ω<br>$R_D$=3.33Ω |
| Rise Time | | $T_r$ | - | 9.6 | - | | |
| Turn-off Delay Time | | $T_{d(off)}$ | - | 52 | - | | |
| Fall Time | | $T_f$ | - | 8.4 | - | | |
| Input Capacitance | | $C_{iss}$ | - | 686 | - | pF | $V_{GS}$=0<br>$V_{DS}$= -15V<br>f=1MHz |
| Output Capacitance | | $C_{oss}$ | - | 90.8 | - | | |
| Reverse Transfer Capacitance | | $C_{rss}$ | - | 80.4 | - | | |
| **Source-Drain Diode** | | | | | | | |
| Forward on Voltage [4] | | $V_{SD}$ | - | -0.7 | -1.2 | V | $I_S$= -1A, $V_{GS}$=0 |
| Continuous Source Current [1] | | $I_S$ | - | - | -3.1 | A | |
| Pulsed Source Current [3] | | $I_{SM}$ | - | - | -12.4 | | |
| Reverse Recovery Time | | $T_{rr}$ | - | 8.4 | - | nS | $I_S$= -3A, $V_{GS}$=0<br>dI/dt=100A/μs |
| Reverse Recovery Charge | | $Q_{rr}$ | - | 3.3 | - | nC | |

Notes:
1. Surface mounted on a 1 inch$^2$ FR-4 board with 2oz copper. t≤5s.
2. Surface mounted on FR-4 Board using the minimum recommended pad size.
3. The power dissipation is limited by 150°C junction temperature, Pw≤300μs, Duty cycle≤1%.
4. The data tested by pulsed, pulse width≤300μs, duty cycle≤2%.

## CHARACTERISTICS CURVE (N-Ch)

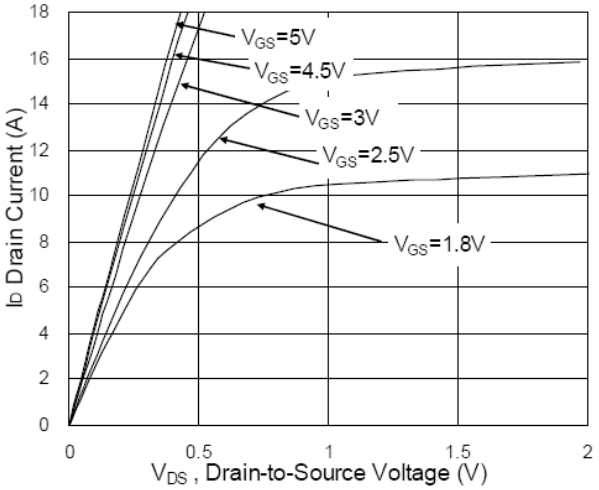



Fig.1 Typical Output Characteristics

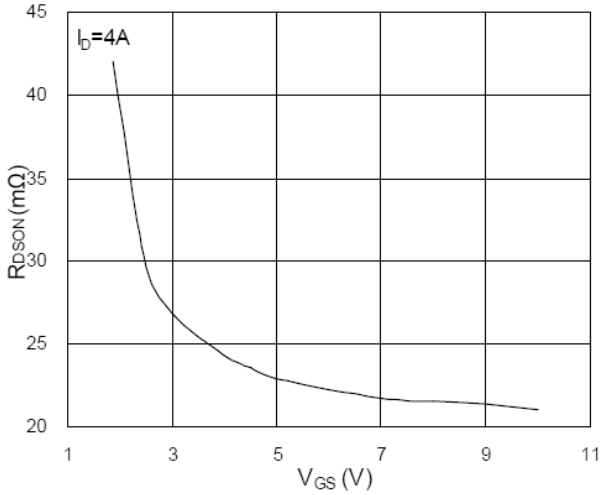



Fig.2 On-Resistance vs. Gate-Source

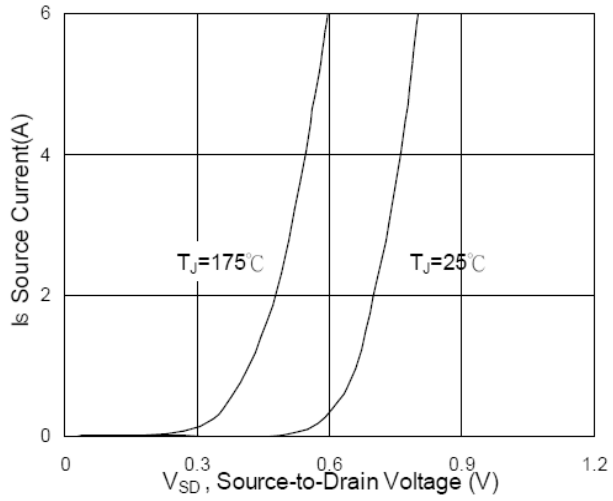



Fig.3 Forward Characteristics Of Reverse

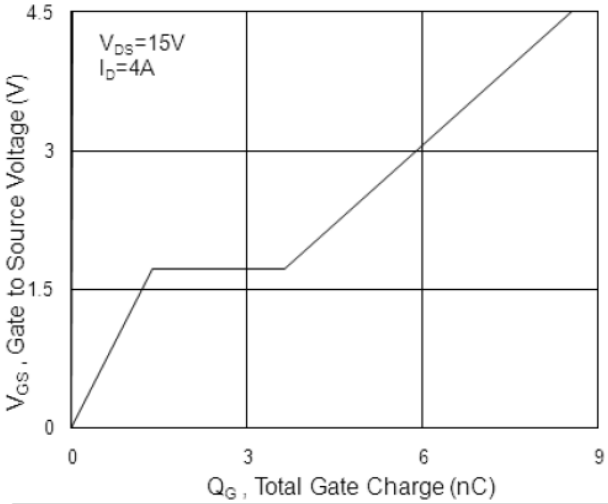



Fig.4 Gate-Charge Characteristics

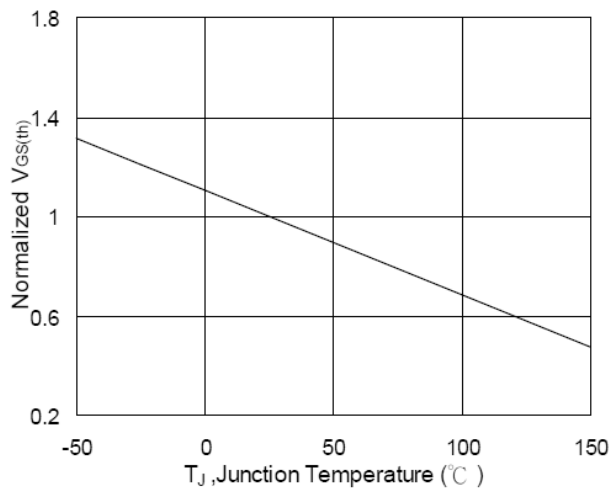



Fig.5 Normalized $V_{GS(th)}$ vs. $T_J$

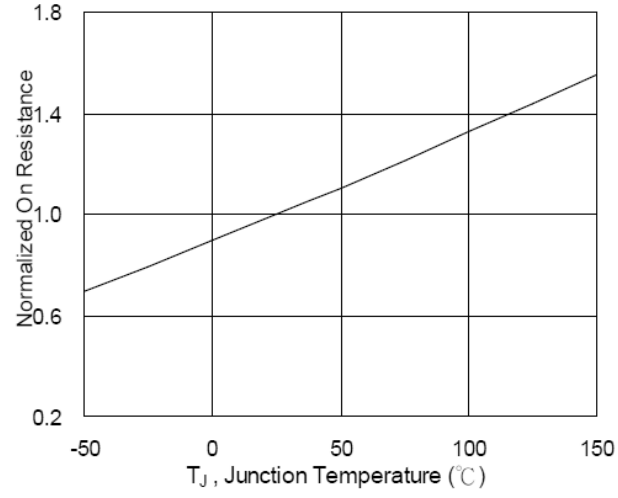



Fig.6 Normalized $R_{DSON}$ vs. $T_J$

## CHARACTERISTICS CURVE (N-Ch)

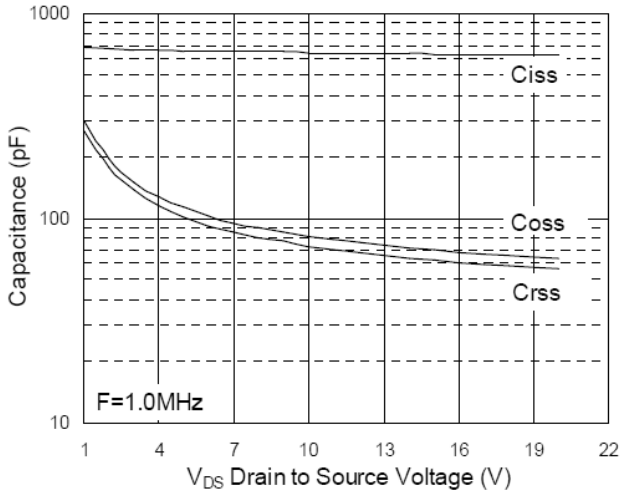



Fig.7 Capacitance

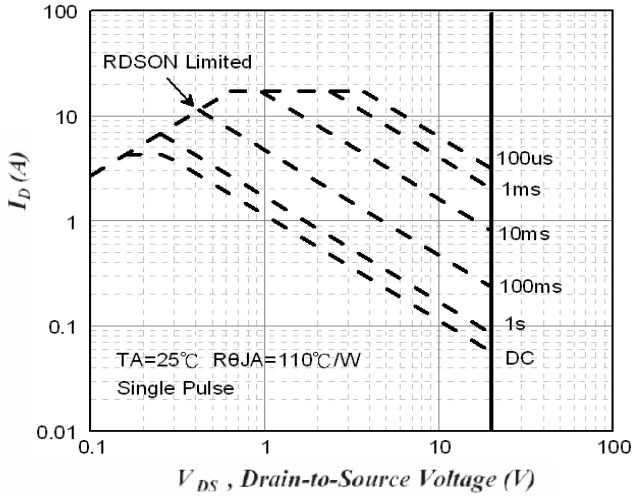



Fig.8 Safe Operating Area

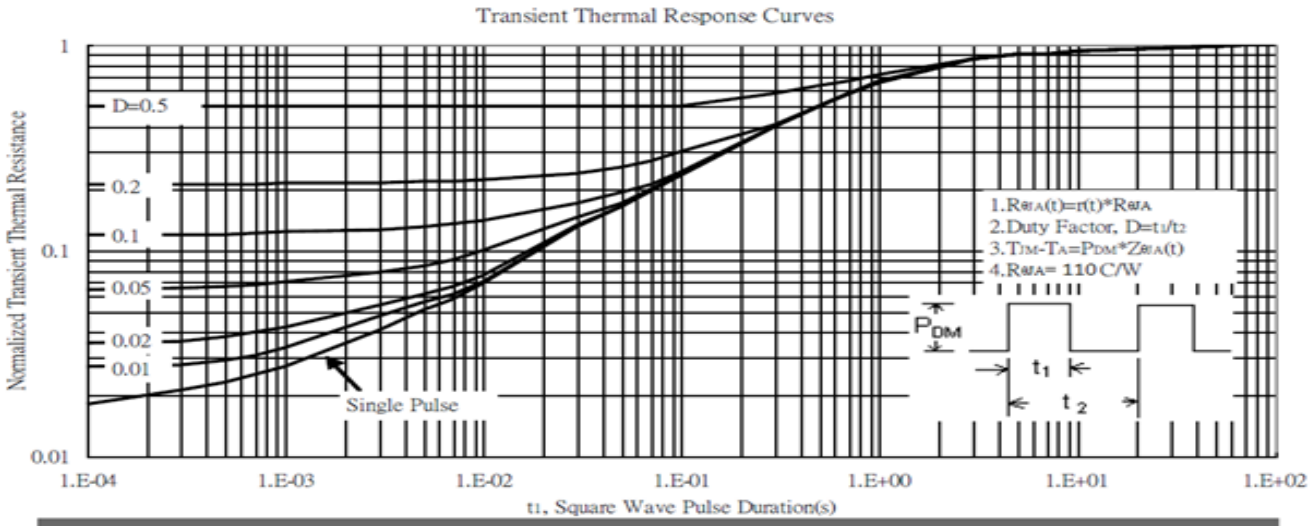



Fig.9 Normalized Maximum Transient Thermal Impedance

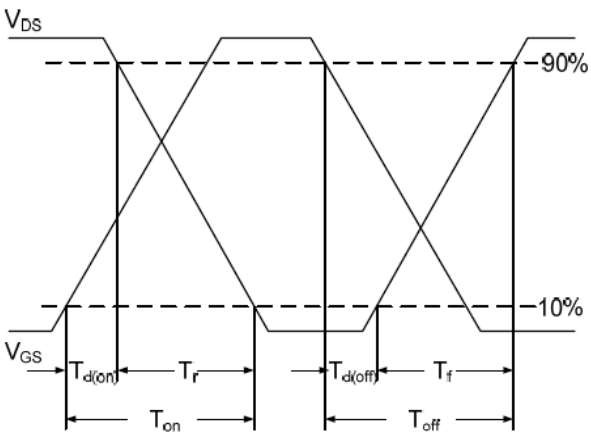



Fig.10 Switching Time Waveform

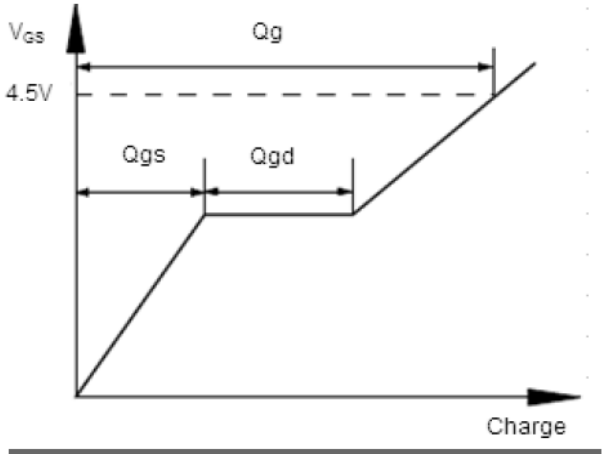



Fig.11 Gate Charge Waveform

## CHARACTERISTICS CURVE (P-Ch)

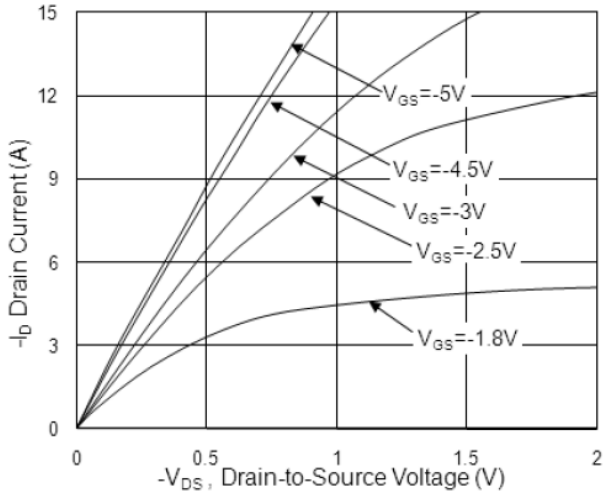



Fig.1 Typical Output Characteristics

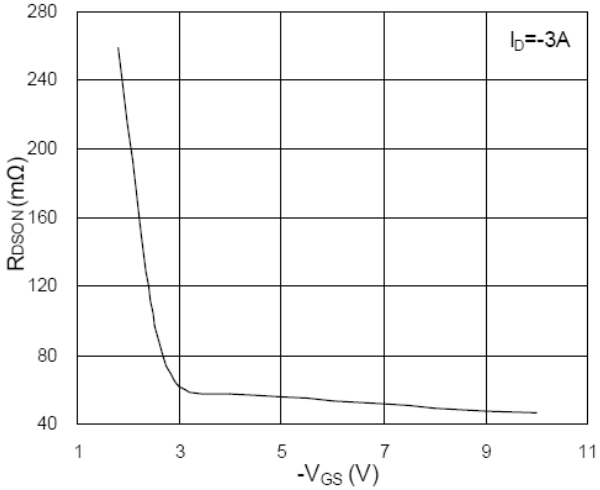



Fig.2 On-Resistance vs. Gate-Source

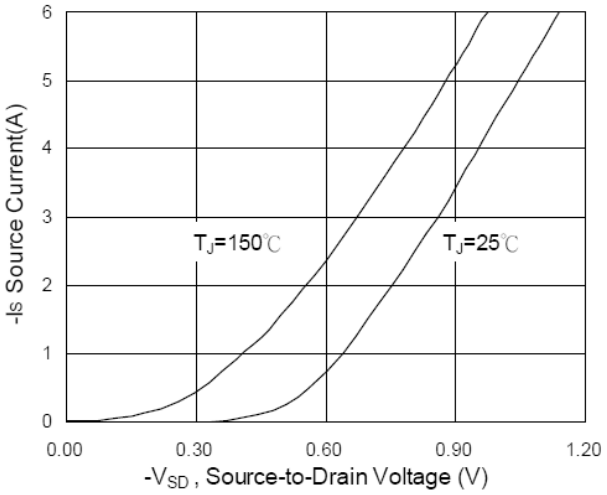



Fig.3 Forward Characteristics Of Reverse

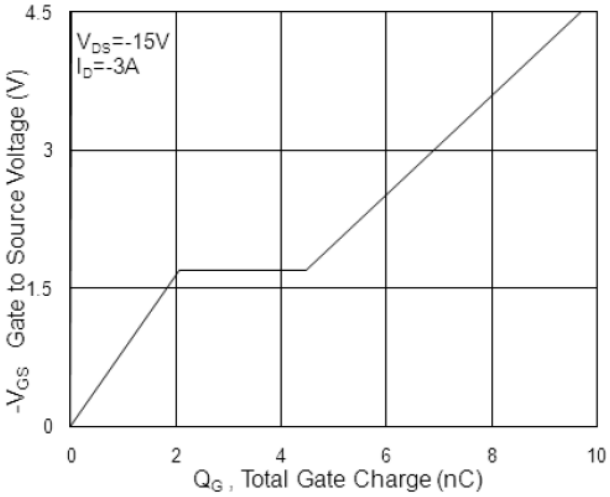



Fig.4 Gate-Charge Characteristics

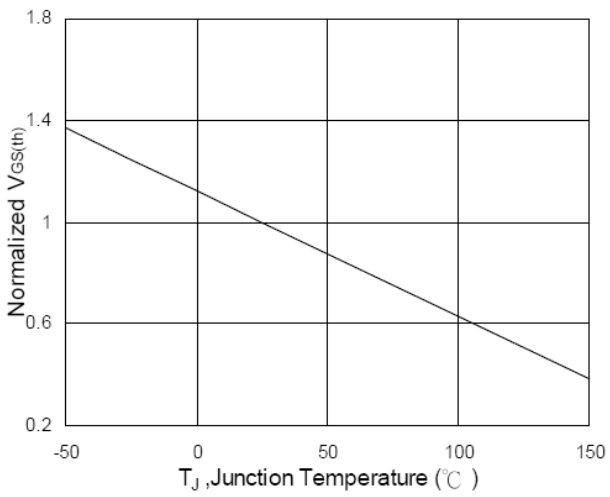



Fig.5 Normalized $V_{GS(th)}$ vs. $T_J$

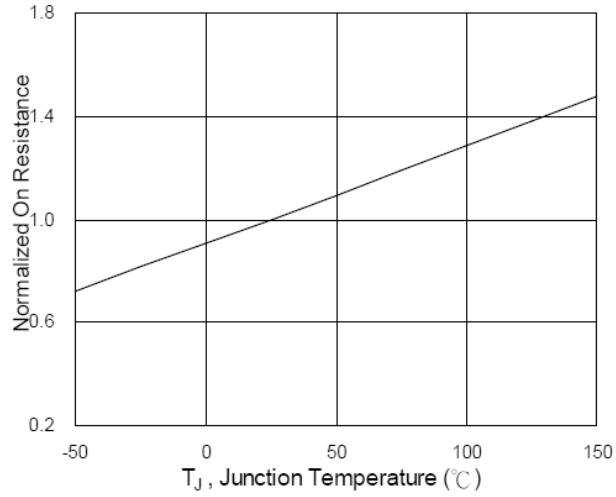



Fig.6 Normalized $R_{DSON}$ vs. $T_J$

## CHARACTERISTICS CURVE (P-Ch)

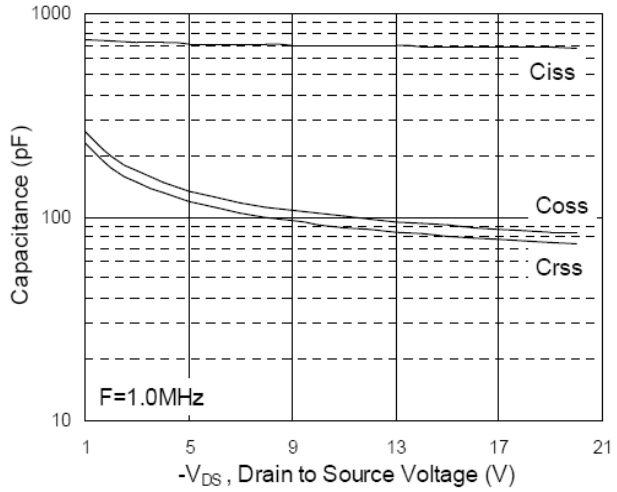



Fig.7 Capacitance

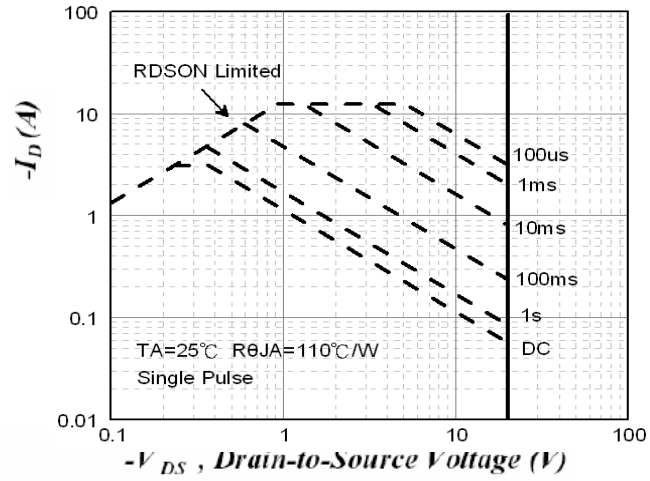



Fig.8 Safe Operating Area

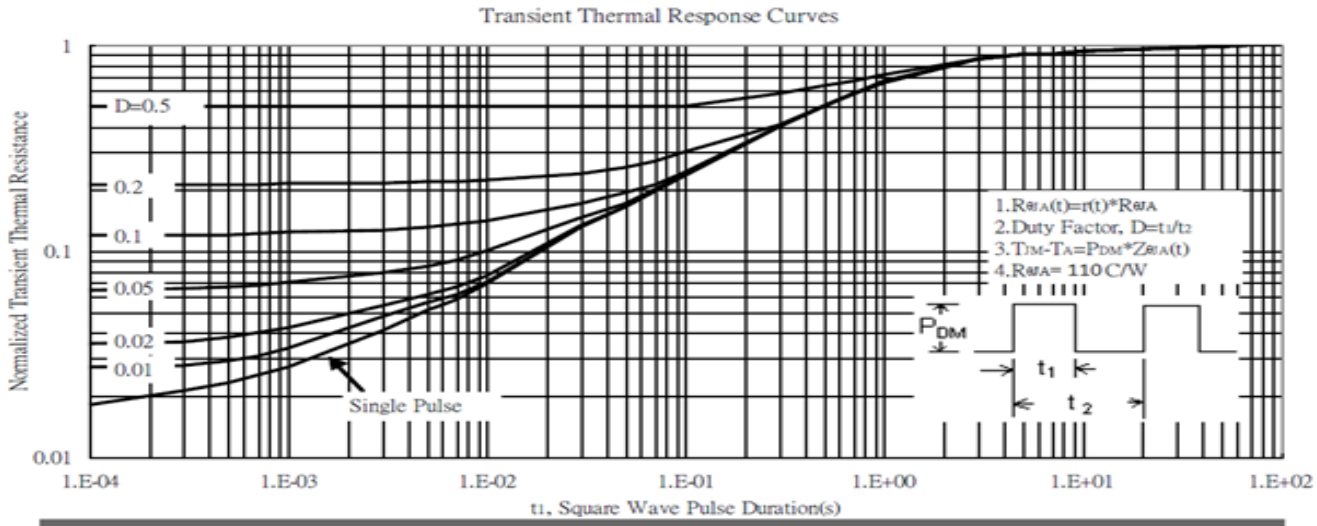



Fig.9 Normalized Maximum Transient Thermal Impedance

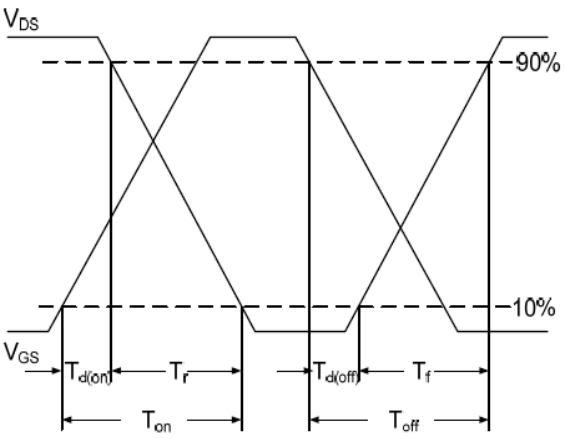



Fig.10 Switching Time Waveform

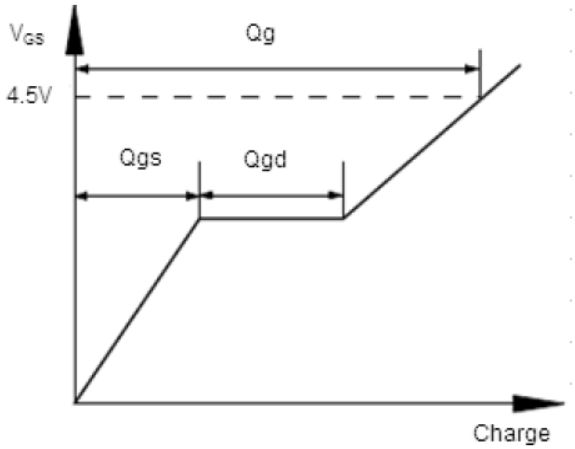



Fig.11 Gate Charge Waveform