Elektronische Bauelemente

SSPR13P10-C

-13A, -100V, $R_{DS(ON)}$ 90mΩ

P-Channel Enhancement Mode Power MOSFET

RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

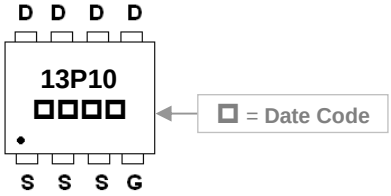
The SSPR13P10-C is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSPR13P10-C meet the RoHS and Green Product requirement with full function reliability approved.

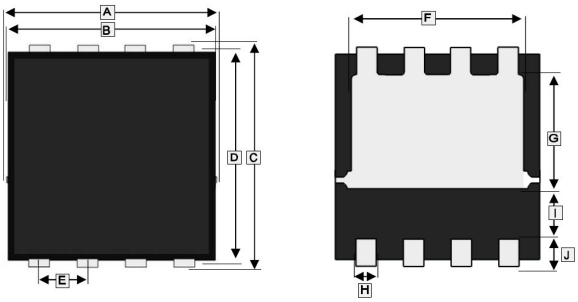
FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING



SPR-8PP



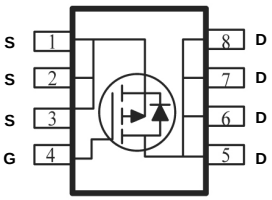
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	3.00	3.40	G	1.35	1.98
B	3.00	3.25	H	0.24	0.35
C	3.20	3.45	I	0.35 TYP.	
D	3.00	3.20	J	0.60 TYP.	
E	0.65 BSC.		K	0.10	0.25
F	2.39	2.60	L	0.70	0.90

PACKAGE INFORMATION

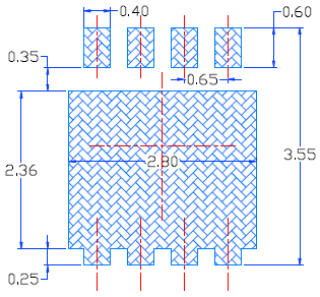
Package	MPQ	Leader Size
SPR-8PP	3K	13 inch

ORDER INFORMATION

Part Number	Type
SSPR13P10-C	Lead (Pb)-free and Halogen-free



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1] @V_{GS}= -10V	T_C=25℃	I_D	-13	A
	T_C=100℃		-7.9	
	T_A=25℃		-3.2	
	T_A=70℃		-2.3	
Pulsed Drain Current [2]		I_{DM}	-50	A
Power Dissipation [1]	T_C=25℃	P_D	34.7	W
	T_C=100℃		13.8	
	T_A=25℃		1.92	
	T_A=70℃		1.23	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Rating				
Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	65	℃/W
Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	3.6	

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	-100	-	-	V	V_{GS}=0, I_D= -250μA
Gate-Threshold Voltage		$V_{GS(th)}$	-1	-	-2.5	V	V_{DS}=V_{GS}, I_D= -250μA
Forward Transconductance		g_{fs}	-	24	-	S	V_{DS}= -10V, I_D= -10A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	-1	μA	V_{DS}= -80V, V_{GS}=0
	T_J=55℃		-	-	-10		
Static Drain-Source On-Resistance [3]		$R_{DS(ON)}$	-	75	90	mΩ	V_{GS}= -10V, I_D= -4.5A
			-	85	110		V_{GS}= -4.5V, I_D= -4A
Total Gate Charge (-4.5V)		Q_g	-	23.2	-	nC	I_D= -13A V_{DS}= -80V V_{GS}= -10V
Total Gate Charge			-	48	-		
Gate-Source Charge		Q_{gs}	-	9.2	-		
Gate-Drain Change		Q_{gd}	-	10	-		
Turn-on Delay Time		$T_{d(on)}$	-	6.2	-	nS	V_{DD}= -50V I_D= -1A V_{GS}= -10V R_G=6Ω
Rise Time		T_r	-	19.2	-		
Turn-off Delay Time		$T_{d(off)}$	-	103	-		
Fall Time		T_f	-	48	-		
Input Capacitance		C_{iss}	-	2914	-	pF	V_{GS}=0 V_{DS}= -25V f=1MHz
Output Capacitance		C_{oss}	-	120	-		
Reverse Transfer Capacitance		C_{rss}	-	58	-		
Source-Drain Diode							
Diode Forward Voltage [3]		V_{SD}	-	-	-1.2	V	I_S= -1A, V_{GS}=0
Continuous Source Current [1]		I_S	-	-	-13	A	
Pulsed Source Current [2]		I_{SM}	-	-	-50	A	
Reverse Recovery Time		T_{rr}	-	38.7	-	nS	I_F= -8A, dI/dt=100A/μs, T_J=25℃
Reverse Recovery Charge		Q_{rr}	-	22.4	-	nC	

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. The power dissipation is limited by 150℃ juncti on temperature.
3. The data tested by pulsed, pulse width≦300us, duty cycle≦2%.

CHARACTERISTIC CURVES

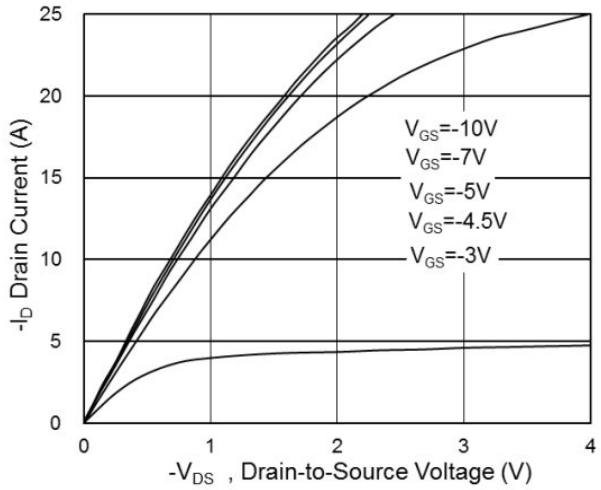


Fig.1 Typical Output Characteristics

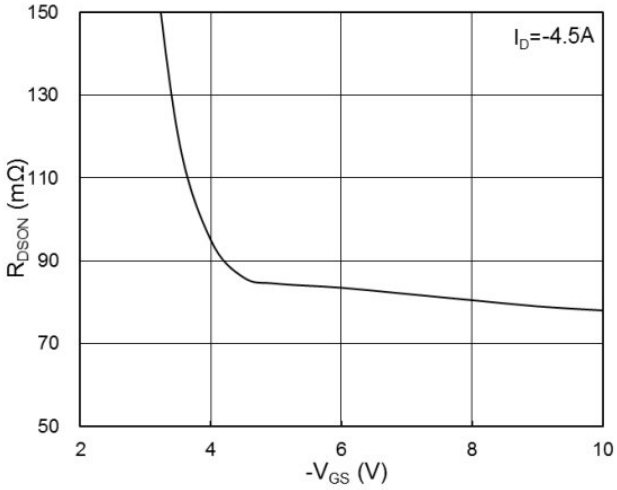


Fig.2 On-Resistance vs G-S Voltage

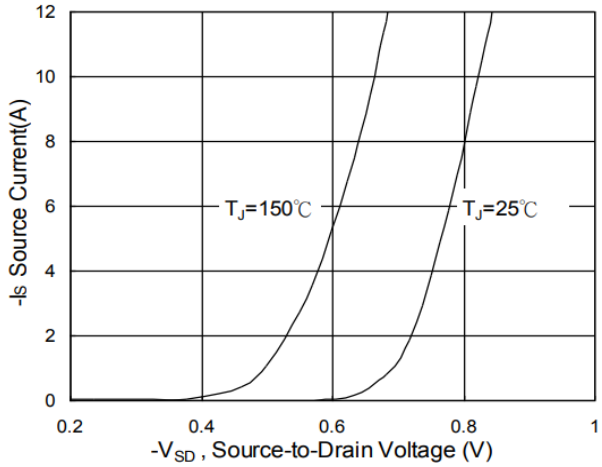


Fig.3 Typical S-D Diode Forward Voltage

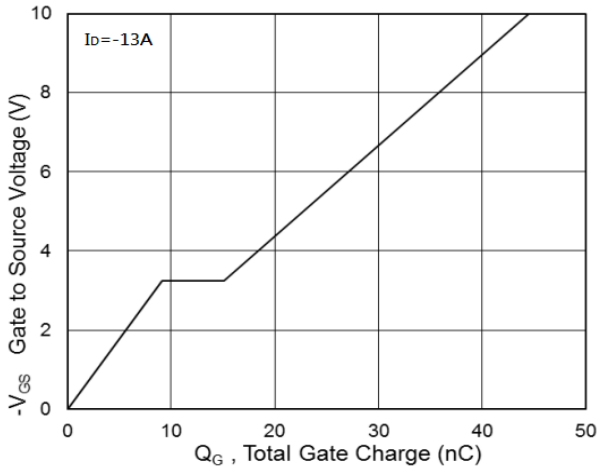


Fig.4 Gate-Charge Characteristics

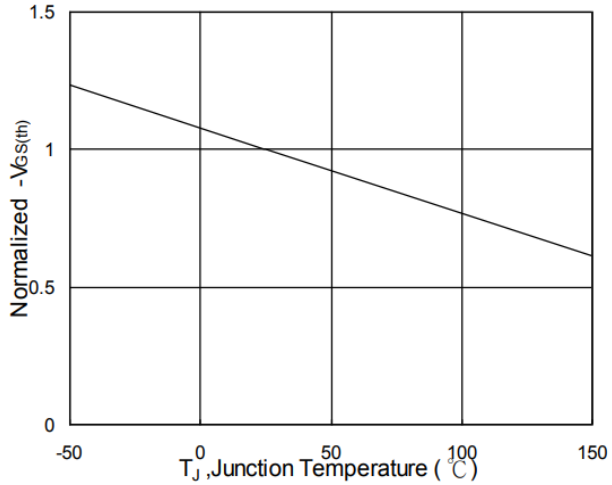


Fig.5 Normalized $V_{GS(th)}$ vs T_J

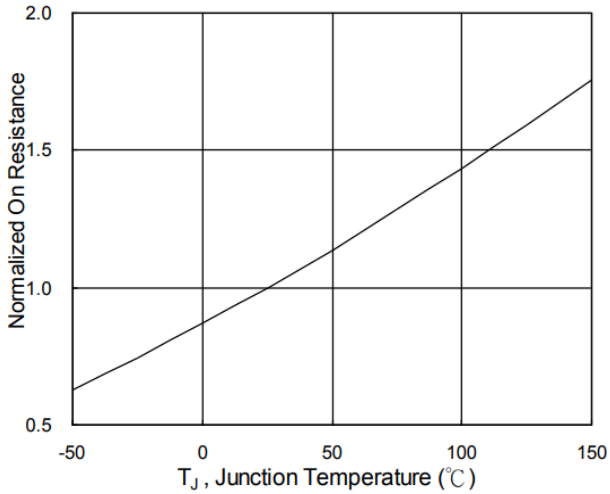


Fig.6 Normalized R_{DSON} vs T_J

CHARACTERISTIC CURVES

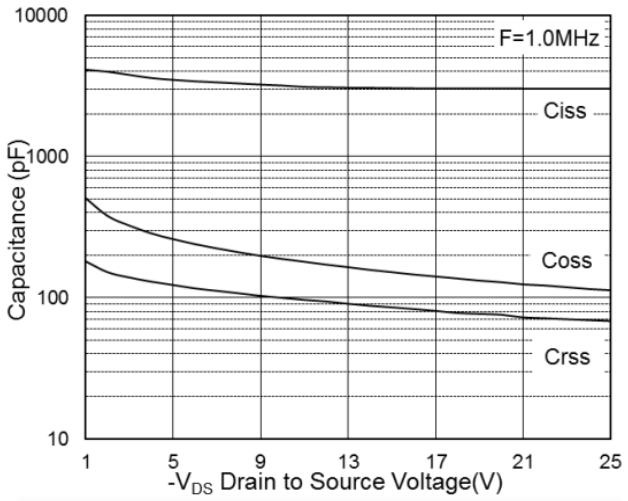


Fig.7 Capacitance

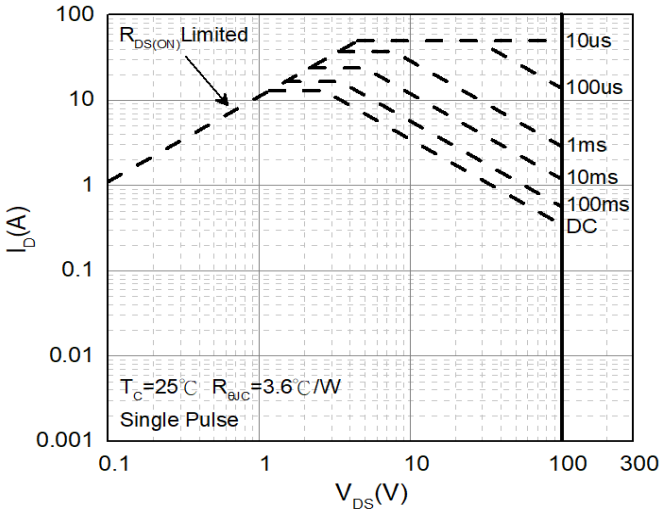


Fig.8 Safe Operating Area

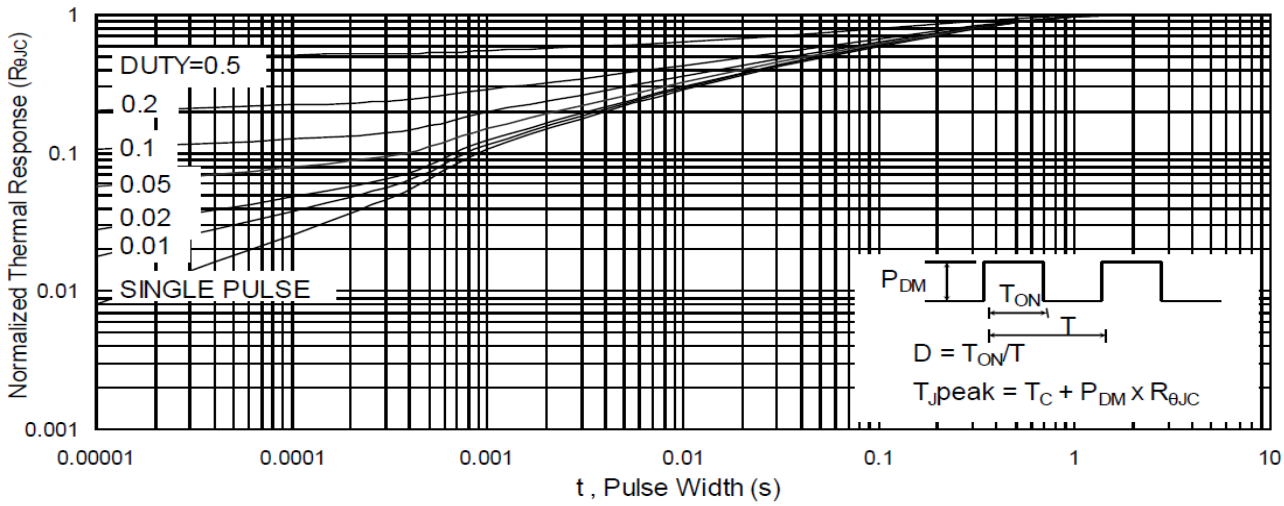


Fig.9 Normalized Maximum Transient Thermal Impedance

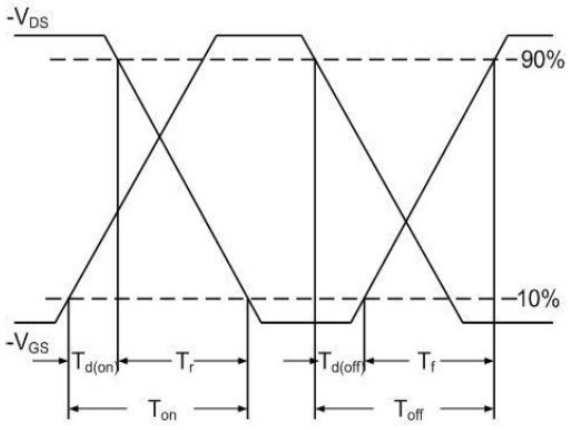


Fig.10 Switching Time Waveform

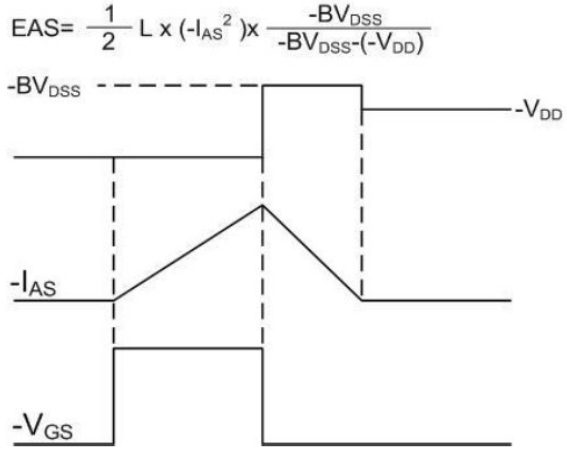


Fig.11 Unclamped Inductive Switching Waveform