Elektronische Bauelemente

SSPR18N10-C

18A, 100V, $R_{DS(ON)}$ 48mΩ

N-Channel Enhancement Mode Power MOSFET

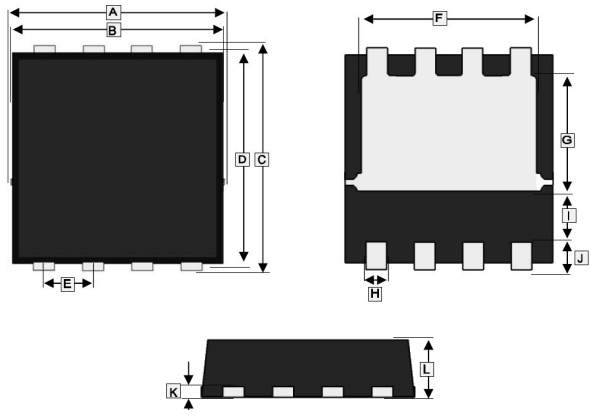
RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SSPR18N10-C provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The SPR-8PP package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

SPR-8PP

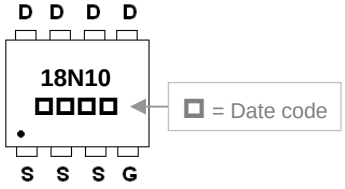


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	3.00	3.40	G	1.35	1.98
B	3.00	3.25	H	0.24	0.35
C	3.20	3.45	I	0.35 TYP.	
D	3.00	3.20	J	0.60 TYP.	
E	0.65 BSC.		K	0.10	0.25
F	2.39	2.60	L	0.70	0.90

FEATURES

- Lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic

MARKING

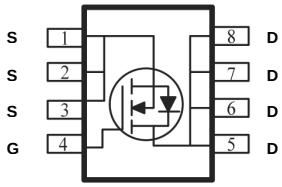


PACKAGE INFORMATION

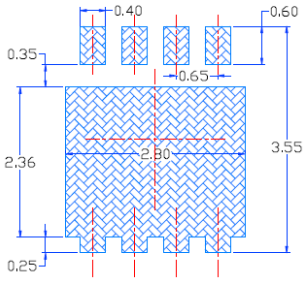
Package	MPQ	Leader Size
SPR-8PP	3K	13 inch

ORDER INFORMATION

Part Number	Type
SSPR18N10-C	Lead (Pb)-free and Halogen-free



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1] @V_{GS}=10V	T_C=25℃	I_D	18	A
	T_C=70℃		11	
Pulsed Drain Current [2]		I_{DM}	52.1	A
Single Pulse Avalanche Energy [3]		E_{AS}	26.6	mJ
Avalanche Current		I_{AS}	20	A
Power Dissipation [4]	T_C=25℃	P_D	34.7	W
Operating Junction & Storage Temperature		T_J, T_{STG}	-55~150	℃
Thermal Resistance Rating				
Thermal Resistance Junction-Ambient [1] (Max.)		$R_{\theta JA}$	50	℃/W
Thermal Resistance Junction-Case [1] (Max.)		$R_{\theta JC}$	3.6	

ELECTRICAL CHARACTERISTICS (T_J = 25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	100	-	-	V	V_{GS}=0, I_D= 250μA
Gate-Threshold Voltage		$V_{GS(th)}$	1	1.7	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	1	μA	V_{DS}=80V, V_{GS}=0
	T_J=55℃		-	-	100		V_{DS}=80V, V_{GS}=0
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	43	48	mΩ	V_{GS}=10V, I_D=18A
			-	45	50		V_{GS}=4.5V, I_D=15A
Gate Resistance		R_g	-	1.6	3.2	Ω	f=1MHz
Total Gate Charge		Q_g	-	61	-	nC	I_D=15A V_{DS}=80V V_{GS}=10V
Gate-Source Charge		Q_{gs}	-	9	-		
Gate-Drain (“Miller”) Change		Q_{gd}	-	10.3	-		
Turn-on Delay Time [2]		$T_{d(on)}$	-	10.8	-	nS	V_{DD}=50V I_D=15A V_{GS}=10V R_G=3.3Ω
Rise Time		T_r	-	48	-		
Turn-off Delay Time		$T_{d(off)}$	-	52	-		
Fall Time		T_f	-	9.6	-		
Input Capacitance		C_{iss}	-	3848	-	pF	V_{GS} =0 V_{DS}=15V f=1MHz
Output Capacitance		C_{oss}	-	137	-		
Reverse Transfer Capacitance		C_{rss}	-	82	-		
Single Pulse Avalanche Energy [5]		E_{AS}	6	-	-	mJ	V_{DD}=25V, L=0.1mH, I_{AS}=10A
Source-Drain Diode							
Diode Forward Voltage [2]		V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0, T_J=25℃
Continuous Source Current [1 6]		I_S	-	-	18	A	V_D=V_G=0, Force Current
Pulsed Source Current [2 6]		I_{SM}	-	-	54	A	
Reverse Recovery Time		T_{rr}	-	29	-	nS	I_F=15A, dI/dt=100A/μs, T_J=25℃
Reverse Recovery Charge		Q_{rr}	-	40	-	nC	

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper, ≦10sec, 125℃/W at steady state.
2. The data tested by pulsed, pulse width≦300us, duty cycle≦2%.
3. The E_{AS} data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=20A.
4. The power dissipation is limited by 150℃ juncti on temperature.
5. The Min. value is 100% E_{AS} tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

CHARACTERISTIC CURVES

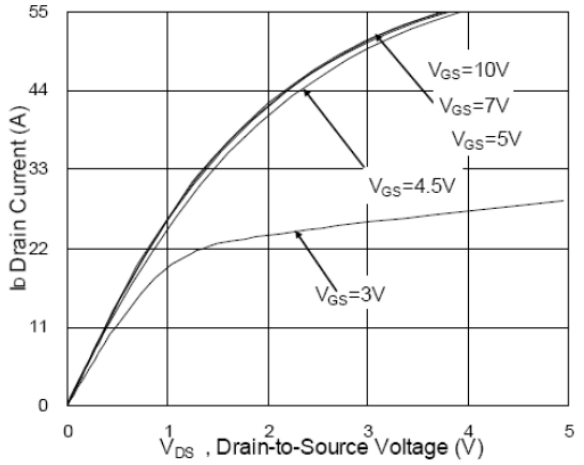


Fig.1 Typical Output Characteristics

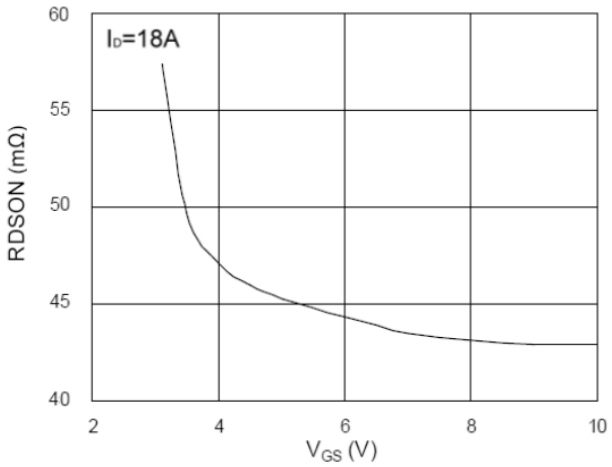


Fig.2 On-Resistance vs. Gate-Source

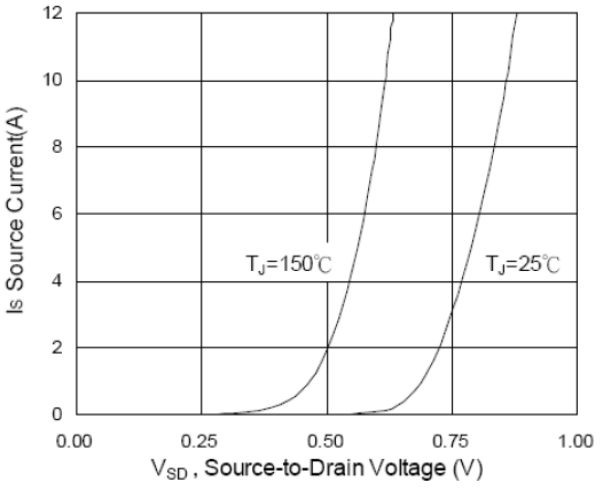


Fig.3 Forward Characteristics Of Reverse

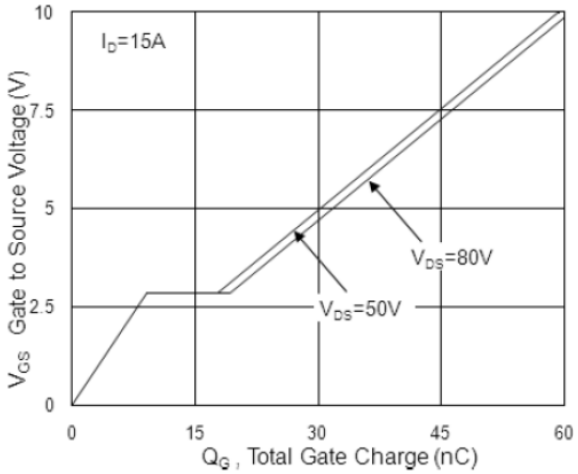


Fig.4 Gate-Charge Characteristics

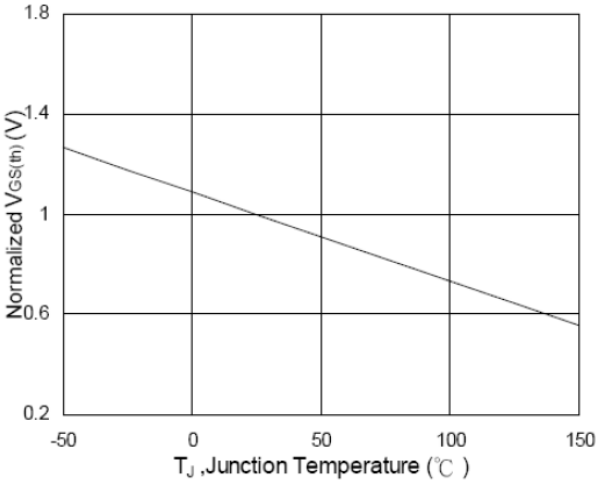


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

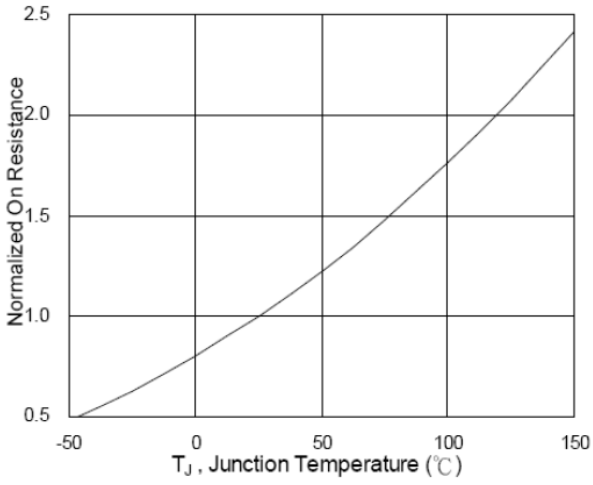


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVES

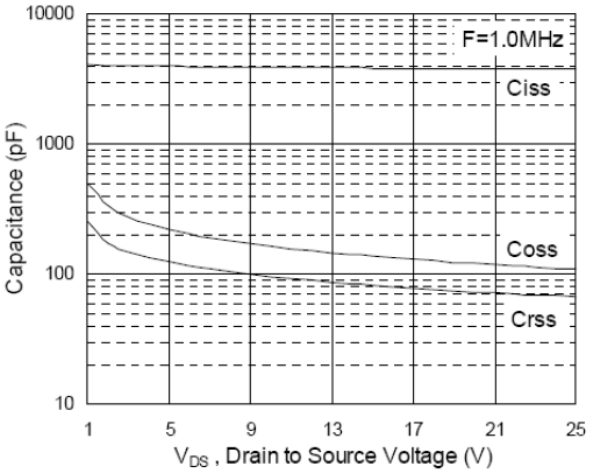


Fig.7 Capacitance

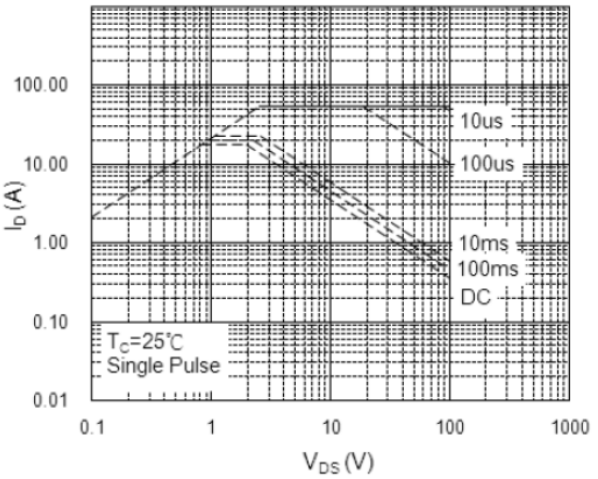


Fig.8 Safe Operating Area

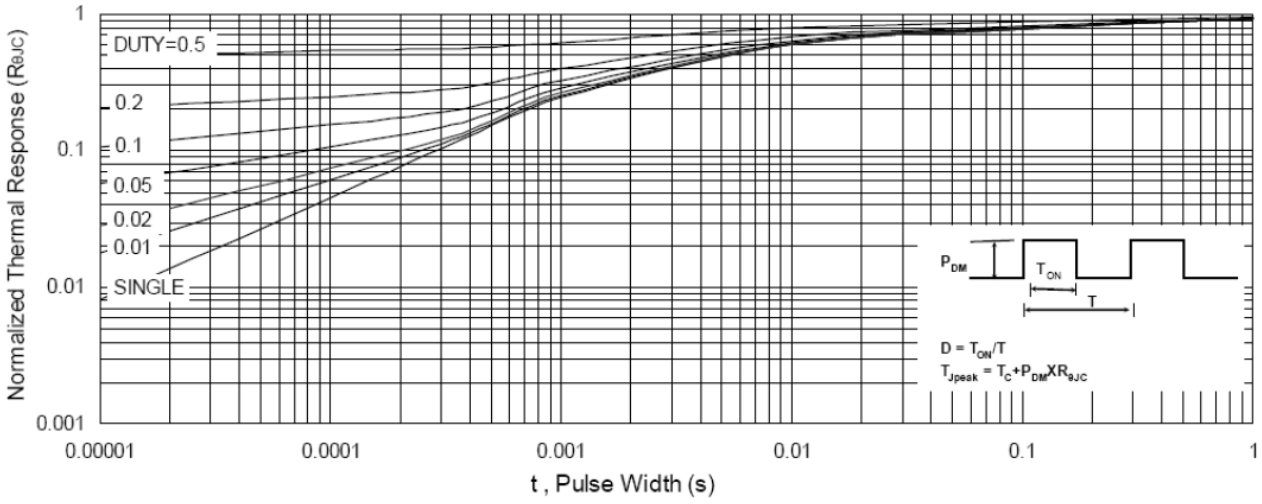


Fig.9 Normalized Maximum Transient Thermal Impedance

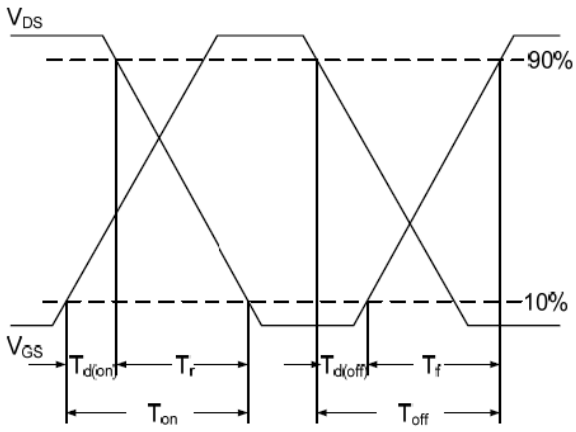


Fig.10 Switching Time Waveform

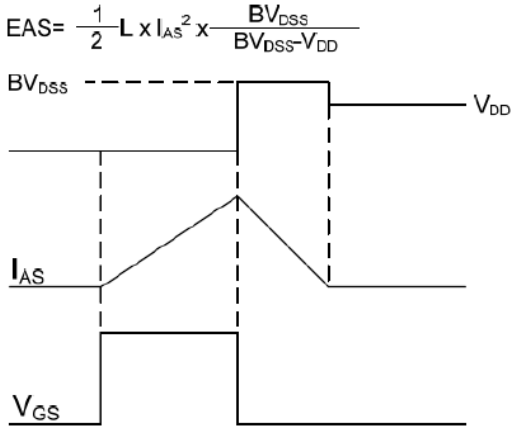


Fig.11 Unclamped Inductive Switching Wave