

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SSRS46N03-C provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

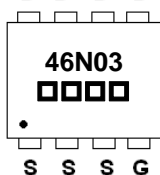
The SPR-8PP package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

FEATURES

- Lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic

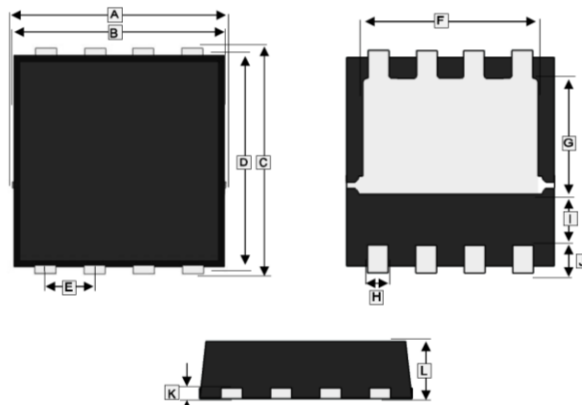
MARKING

D D D D



□ = Date code

SPR-8PP



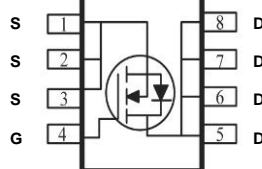
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	3.00	3.40	G	1.35	1.98
B	3.00	3.25	H	0.24	0.35
C	3.20	3.45	I	0.35 TYP.	
D	3.00	3.20	J	0.60 TYP.	
E	0.65 BSC.		K	0.10	0.25
F	2.39	2.60	L	0.70	0.90

PACKAGE INFORMATION

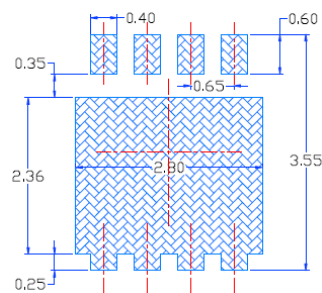
Package	MPQ	Leader Size
SPR-8PP	3K	13 inch

ORDER INFORMATION

Part Number	Type
SSPR46N03-C	Lead (Pb)-free and Halogen-free



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹ @ $V_{GS}=10\text{V}$	I_D	$T_C=25^\circ\text{C}$	46
		$T_C=100^\circ\text{C}$	29
		$T_A=25^\circ\text{C}$	11
		$T_A=70^\circ\text{C}$	9
Pulsed Drain Current ²	I_{DM}	92	A
Single Pulse Avalanche Energy ³	E_{AS}	57.8	mJ
Avalanche Current	I_{AS}	34	A
Power Dissipation ⁴	P_D	$T_C=25^\circ\text{C}$	29
		$T_A=25^\circ\text{C}$	1.67
Operating Junction & Storage Temperature	T_J, T_{STG}	55~150	$^\circ\text{C}$
Thermal Resistance Rating			
Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	75	$^\circ\text{C/W}$
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	4.32	

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ C$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS}=0, I_D=250\mu A$	
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$	
Forward Transconductance	g_{fs}	-	9.8	-	S	$V_{DS}=5V, I_D=15A$	
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0$	
Drain-Source Leakage Current	I_{DSS}	$T_J=25^\circ C$	-	-	1	μA	$V_{DS}=24V, V_{GS}=0$
		$T_J=55^\circ C$	-	-	5		
Static Drain-Source On-Resistance ²	$R_{DS(ON)}$	-	-	9	m Ω	$V_{GS}=10V, I_D=12A$	
		-	-	15		$V_{GS}=4.5V, I_D=10A$	
Gate Resistance	R_g	-	2.6	-	Ω	$f=1MHz$	
Total Gate Charge	Q_g	-	10.1	-	nC	$I_D=12A$ $V_{DS}=20V$ $V_{GS}=4.5V$	
Gate-Source Charge	Q_{gs}	-	3.6	-			
Gate-Drain Charge	Q_{gd}	-	4.3	-			
Turn-on Delay Time ²	$T_{d(on)}$	-	6.1	-	nS	$V_{DD}=12V$ $I_D=5A$ $V_{GS}=10V$ $R_G=3.3\Omega$	
Rise Time	T_r	-	2.5	-			
Turn-off Delay Time	$T_{d(off)}$	-	20.7	-			
Fall Time	T_f	-	4	-			
Input Capacitance	C_{iss}	-	1118	-	pF	$V_{GS}=0$ $V_{DS}=15V$ $f=1MHz$	
Output Capacitance	C_{oss}	-	173	-			
Reverse Transfer Capacitance	C_{rss}	-	94	-			
Source-Drain Diode							
Diode Forward Voltage ²	V_{SD}	-	-	1	V	$I_S=1A, V_{GS}=0, T_J=25^\circ C$	
Continuous Source Current ^{1 5}	I_S	-	-	46	A	$V_D=V_G=0, \text{Force Current}$	
Pulsed Source Current ^{2 5}	I_{SM}	-	-	92	A		

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. The E_{AS} data shows Max. rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=34A$.
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

CHARACTERISTIC CURVES

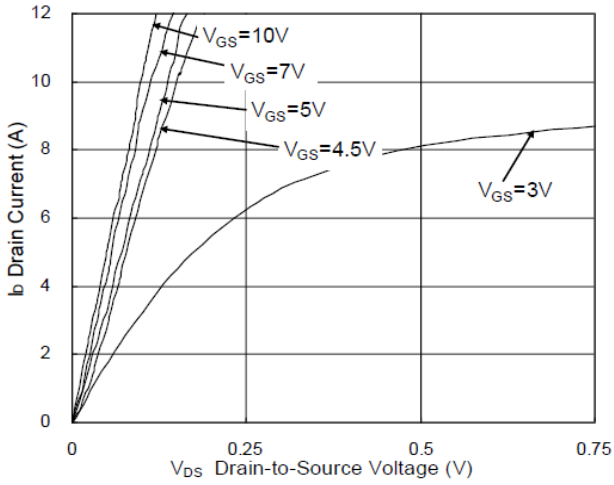


Fig.1 Typical Output Characteristics

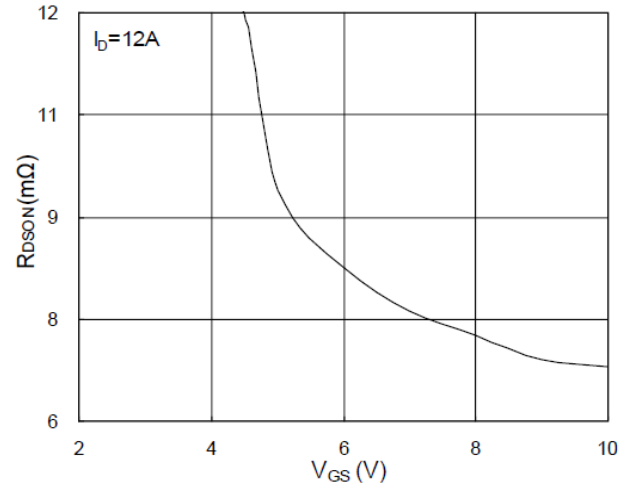


Fig.2 On-Resistance vs. Gate-Source

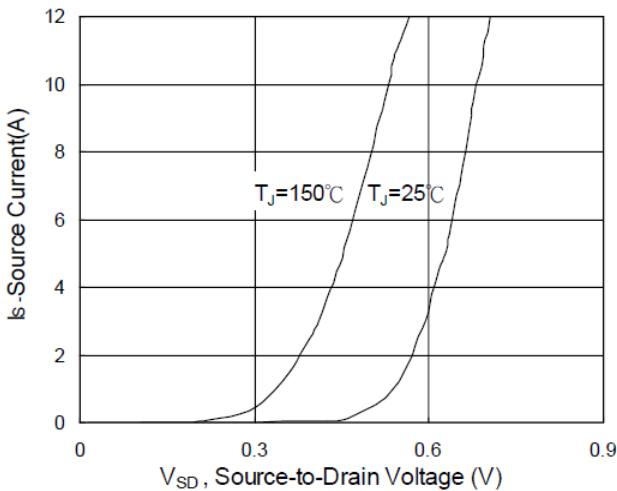


Fig.3 Forward Characteristics Of Reverse

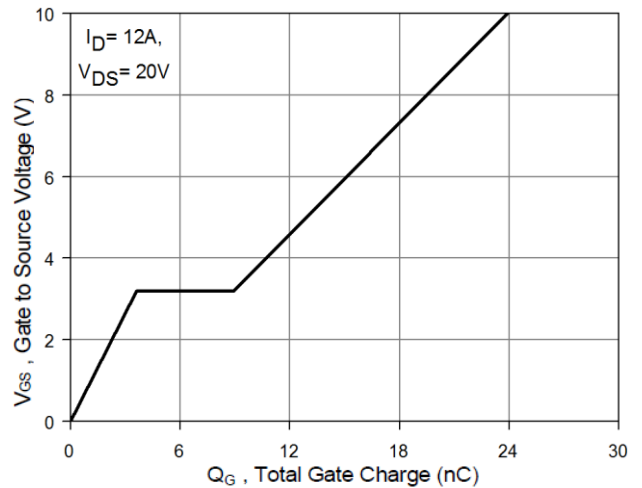


Fig.4 Gate-Charge Characteristics

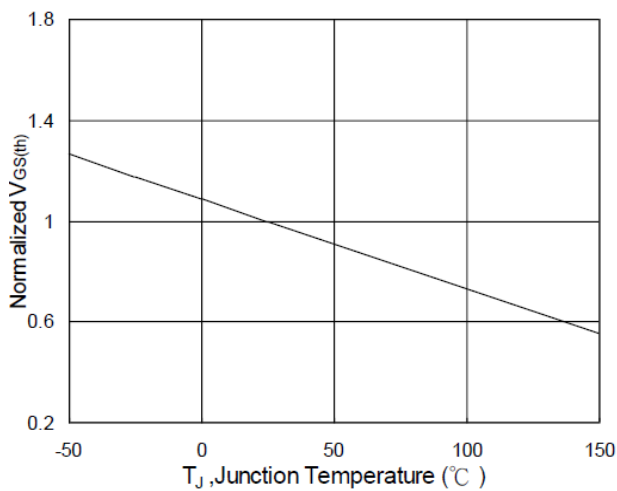


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

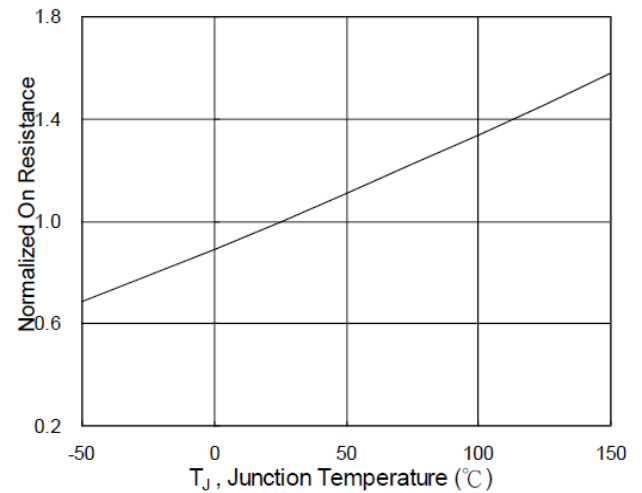


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

CHARACTERISTIC CURVES

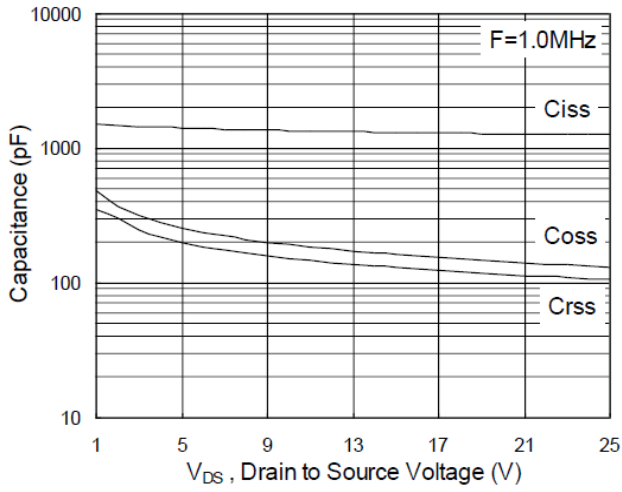


Fig.7 Capacitance

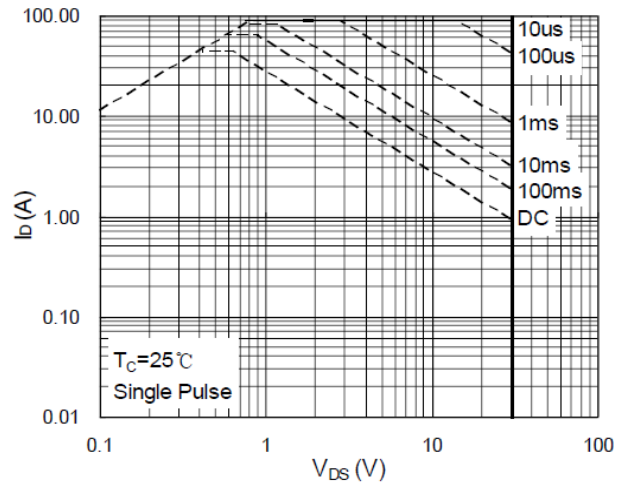


Fig.8 Safe Operating Area

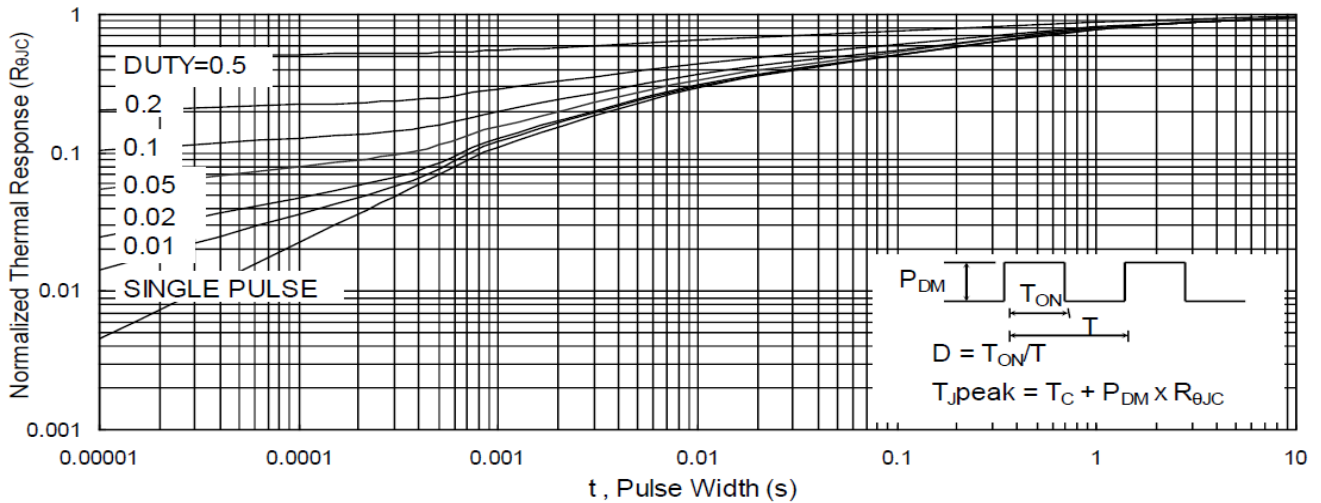


Fig.9 Normalized Maximum Transient Thermal Impedance

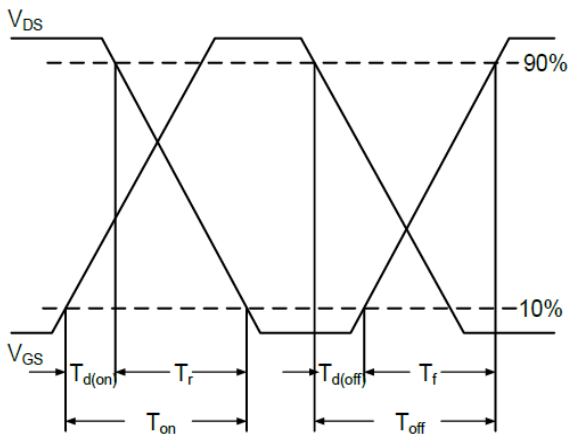


Fig.10 Switching Time Waveform

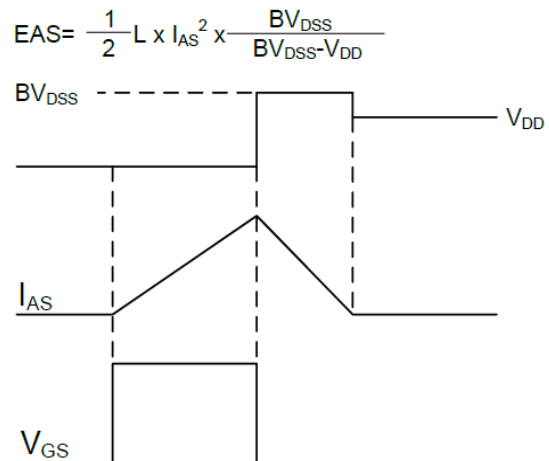


Fig.11 Unclamped Inductive Switching Waveform