

RoHS Compliant Product  
A suffix of "-C" specifies halogen & lead-free

## DESCRIPTION

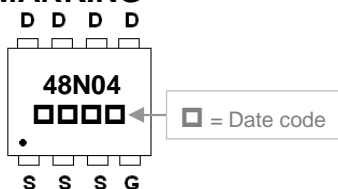
The SSPR48N04-C is the highest performance trench N-Ch MOSFETs with extreme high cell density, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the synchronous buck converter applications.

The SSPR48N04-C meet the RoHS and Green Product requirement with full function reliability approved.

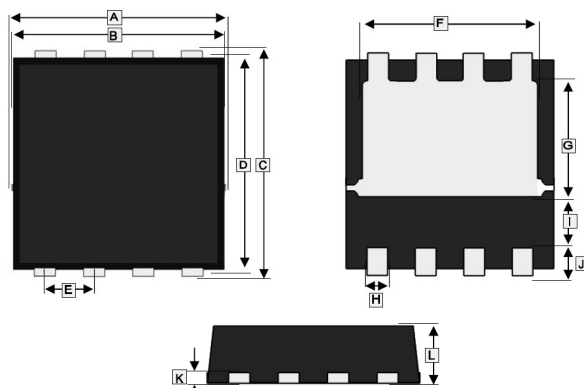
## FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge

## MARKING



## SPR-8PP



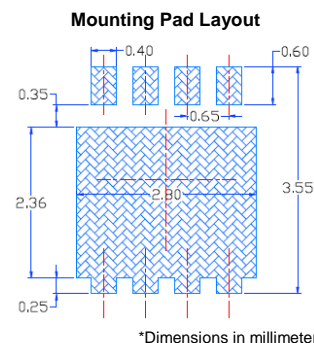
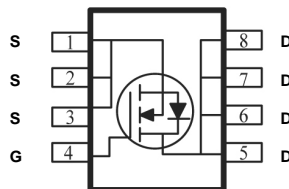
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	3.00	3.40	G	1.35	1.98
B	3.00	3.25	H	0.24	0.35
C	3.20	3.45	I	0.35 TYP.	
D	3.00	3.20	J	0.60 TYP.	
E	0.65 BSC.		K	0.10	0.25
F	2.39	2.60	L	0.70	0.90

## PACKAGE INFORMATION

Package	MPQ	Leader Size
SPR-8PP	3K	13 inch

## ORDER INFORMATION

Part Number	Type
SSPR48N04-C	Lead (Pb)-free and Halogen-free



## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup> @ $V_{GS}=10V$	$I_D$	$T_C=25^\circ C$	48
		$T_C=100^\circ C$	36
		$T_A=25^\circ C$	11
		$T_A=70^\circ C$	8.8
Pulsed Drain Current <sup>3</sup>	$I_{DM}$	100	A
Total Power Dissipation	$P_D$	$T_C=25^\circ C$	32
		$T_A=25^\circ C$	1.67
Operating Junction & Storage Temperature	$T_J, T_{STG}$	-55~150	$^\circ C$
Thermal Resistance Ratings			
Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	75	$^\circ C/W$
Thermal Resistance Junction-Ambient <sup>2</sup>		135	
Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	3.9	

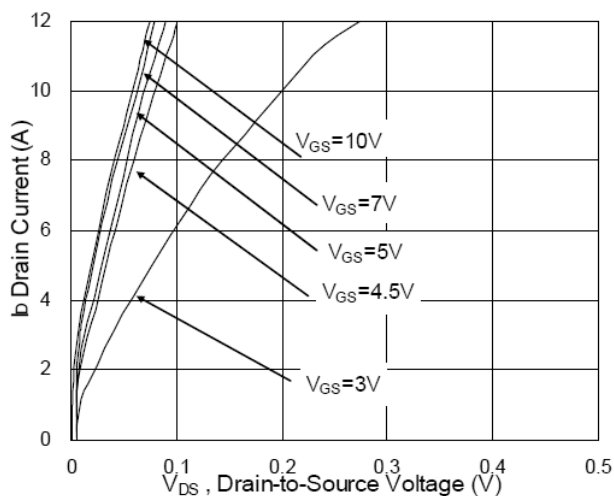
**ELECTRICAL CHARACTERISTICS** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Drain-Source Breakdown Voltage	$BV_{DSS}$	40	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$	
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	
Forward Transconductance	$g_{fs}$	-	39	-	S	$V_{DS}=5\text{V}, I_D=12\text{A}$	
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 20\text{V}$	
Drain-Source Leakage Current	$I_{DSS}$	$T_J=25^\circ\text{C}$	-	-	1	$\mu\text{A}$	$V_{DS}=32\text{V}, V_{GS}=0$
		$T_J=55^\circ\text{C}$	-	-	5		$V_{DS}=32\text{V}, V_{GS}=0$
Static Drain-Source On-Resistance <sup>4</sup>	$R_{DS(ON)}$	-	-	8.5	m $\Omega$	$V_{GS}=10\text{V}, I_D=12\text{A}$	
		-	-	10		$V_{GS}=4.5\text{V}, I_D=10\text{A}$	
Total Gate Charge	$Q_g$	-	18.8	-	nC	$I_D=12\text{A}$ $V_{DS}=20\text{V}$ $V_{GS}=4.5\text{V}$	
Gate-Source Charge	$Q_{gs}$	-	4.7	-			
Gate-Drain ("Miller") Charge	$Q_{gd}$	-	8.2	-			
Turn-on Delay Time	$T_{d(on)}$	-	14.3	-	nS	$V_{DD}=15\text{V}$ $I_D=1\text{A}$ $V_{GS}=10\text{V}$ $R_G=3.3\Omega$	
Rise Time	$T_r$	-	2.6	-			
Turn-off Delay Time	$T_{d(off)}$	-	77	-			
Fall Time	$T_f$	-	4.8	-			
Input Capacitance	$C_{iss}$	-	2332	-	pF	$V_{GS}=0$ $V_{DS}=15\text{V}$ $f=1\text{MHz}$	
Output Capacitance	$C_{oss}$	-	193	-			
Reverse Transfer Capacitance	$C_{rss}$	-	138	-			
<b>Source-Drain Diode</b>							
Diode Forward Voltage <sup>4</sup>	$V_{SD}$	-	-	1.2	V	$I_S=1\text{A}, V_{GS}=0$	
Continuous Source Current <sup>1</sup>	$I_S$	-	-	48	A		
Pulsed Source Current <sup>3</sup>	$I_{SM}$	-	-	100	A		

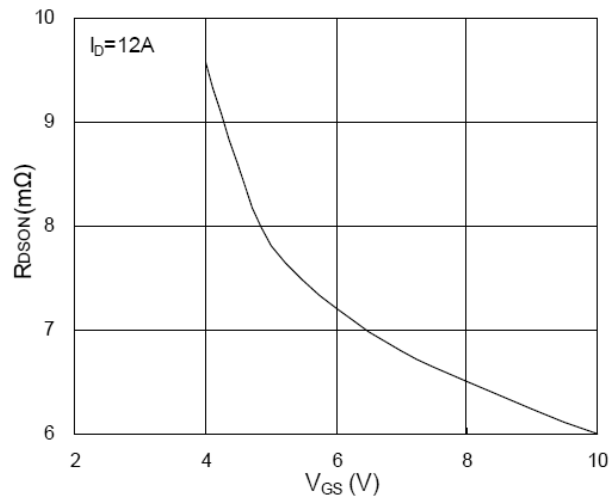
Notes:

1. Surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2oz copper.
2. When mounted on Min. Copper pad.
3. Pulse width limited by maximum junction temperature, pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
4. The data tested by pulsed, pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .

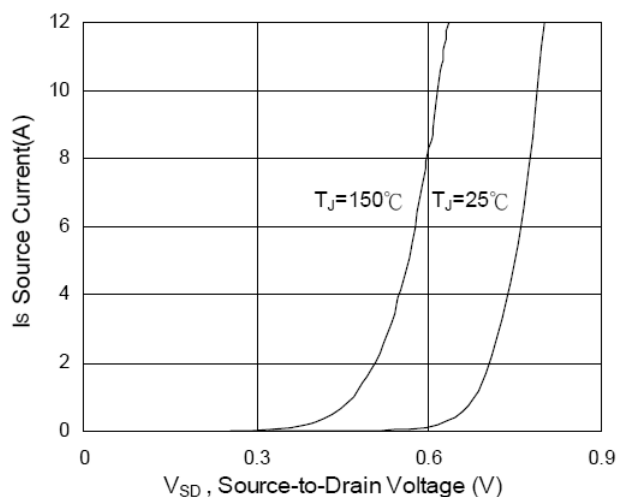
**CHARACTERISTIC CURVES**



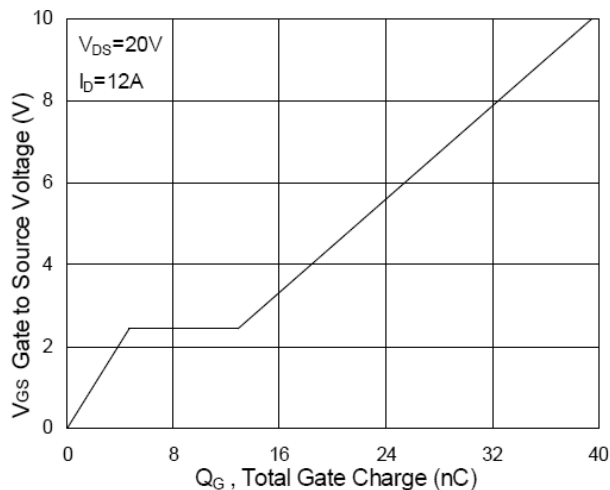
**Fig.1 Typical Output Characteristics**



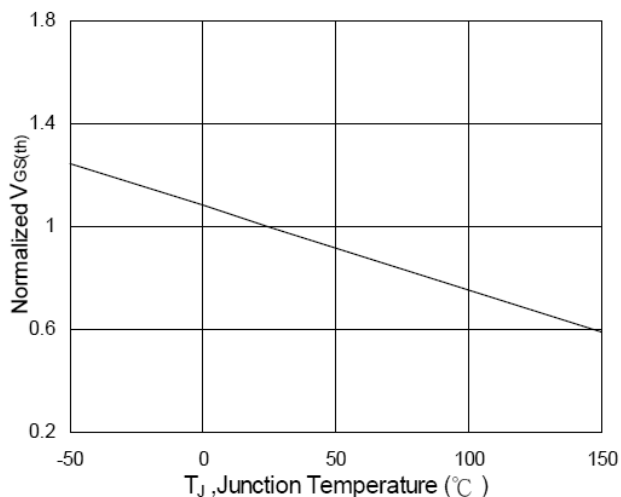
**Fig.2 On-Resistance vs. G-S Voltage**



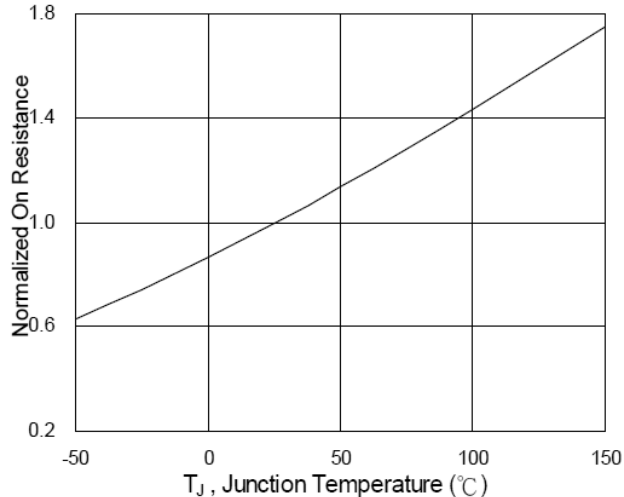
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

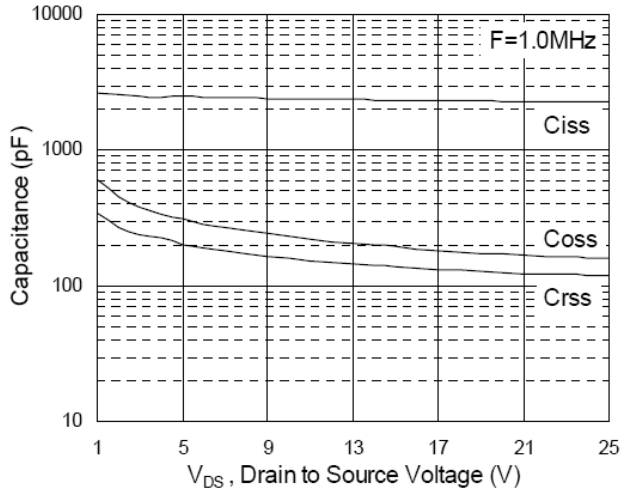


**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**

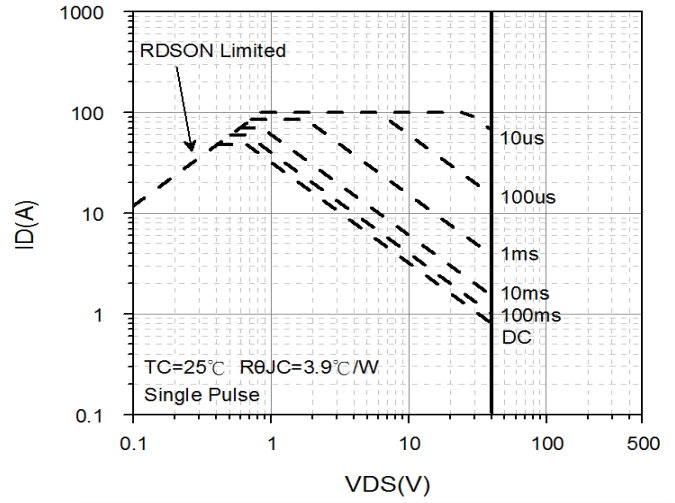


**Fig.6 Normalized  $R_{DS(ON)}$  vs.  $T_J$**

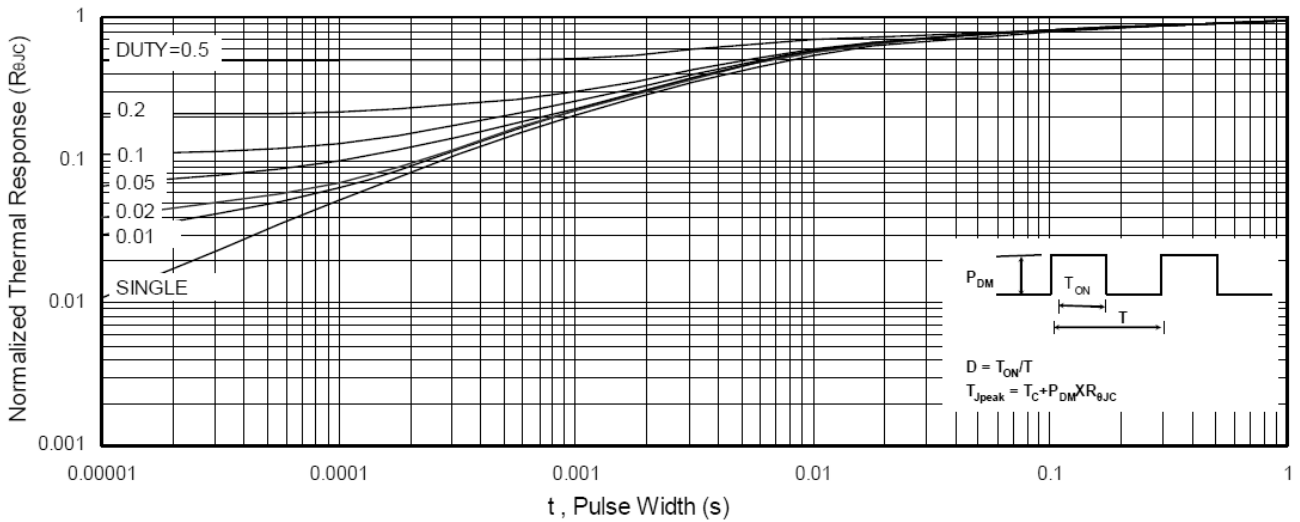
**CHARACTERISTIC CURVES**



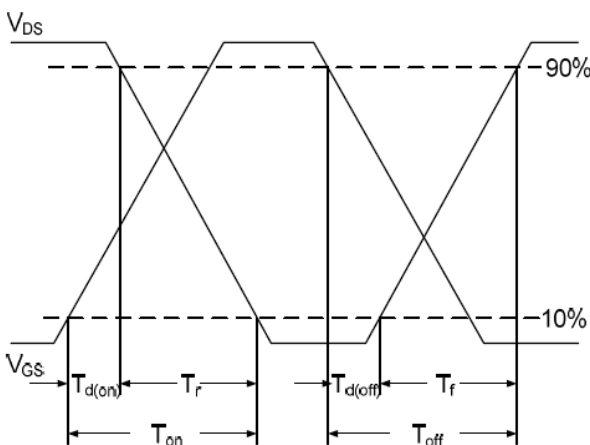
**Fig.7 Capacitance**



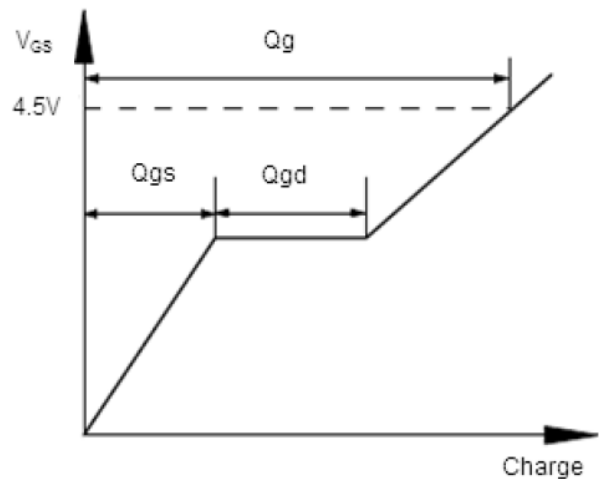
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**