Elektronische Bauelemente

SSE50N10-C

54A, 100V, $R_{DS(ON)}$ 20mΩ

N-Ch Enhancement Mode Power MOSFET

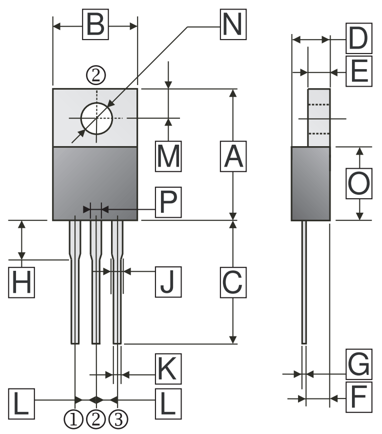
RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSE50N10-C is the highest performance trench N-Ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSE50N10-C meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO-220



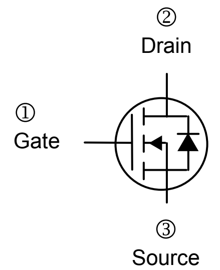
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	14.22	16.51	J	0.70	1.78
B	9.57	10.90	K	0.38	1.11
C	12.50	14.75	L	2.01	3.07
D	3.56	5.10	M	2.22	3.43
E	0.51	1.47	N	3.10	4.31
F	2.03	3.19	O	8.10	9.65
G	0.279	0.76	P	1.18 Typ.	
H	2.95	4.5			

FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available

MARKING

50N10
□□□□ ← Date Code



ORDER INFORMATION

Part Number	Type
SSE50N10-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1], @V_{GS}=10V	T_C=25°C	I_D	54	A
	T_C=100°C		38	
Pulsed Drain Current [2]	T_C=25°C	I_{DM}	130	A
Single Pulse Avalanche Energy [3]		EAS	312	mJ
Avalanche Current		I_{AS}	25	A
Total Power Dissipation	T_C=25°C	P_D	104	W
	T_A=25°C		2	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	°C
Thermal Data				
Maximum Thermal Resistance Junction-Case [1]		$R_{θJC}$	1.2	°C/W
Maximum Thermal Resistance Junction-Ambient [1]		$R_{θJA}$	62.5	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	100	-	-	V	V_{GS}=0, I_D=250μA
Gate Threshold Voltage		$V_{GS(th)}$	2	-	4	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	1	μA	V_{DS}=80V, V_{GS}=0
	T_J=55°C		-	-	5		V_{DS}=80V, V_{GS}=0
Static Drain-Source On-Resistance [4]		$R_{DS(ON)}$	-	14	20	mΩ	V_{GS}=10V, I_D=30A
Total Gate Charge		Q_g	-	27.6	-	nC	I_D=30A V_{DS}=80V V_{GS}=10V
Gate-Source Charge		Q_{gs}	-	11.4	-		
Gate-Drain Change		Q_{gd}	-	7.9	-		
Turn-on Delay Time		$T_{d(on)}$	-	16.5	-	nS	V_{DS}=50V I_D=30A V_{GS}=10V R_L=3.3Ω
Rise Time		T_r	-	35	-		
Turn-off Delay Time		$T_{d(off)}$	-	17.5	-		
Fall Time		T_f	-	12	-		
Input Capacitance		C_{iss}	-	1890	-	pF	V_{GS}=0 V_{DS}=15V f=1MHz
Output Capacitance		C_{oss}	-	268	-		
Reverse Transfer Capacitance		C_{rss}	-	67	-		
Gate Resistance		R_g	-	1.9	3.8	Ω	f=1MHz
Guaranteed Avalanche Chatacteristics							
Single Pulse Avalanche Energy [5]		E_{AS}	84.5	-	-	mJ	V_{DD}=50V, L=1mH, I_{AS}=13A
Source-Drain Diode							
Continuous Source Current [1,6]		I_S	-	-	54	A	
Pulsed Source Current [2,6]		I_{SM}	-	-	130		
Diode Forward Voltage [4]		V_{SD}	-	-	1.2	V	V_{GS}=0, I_S=1A, T_J=25°C
Reverse Recovery Time		t_{rr}	-	34	-	nS	I_F=30A, dI/dt=100A/μs T_J=25°C
Reverse Recovery Charge		Q_{rr}	-	47	-	nC	

Notes:
1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. Pulse width limited by maximum junction temperature, Pulse Width≦300μs, Duty Cycle≦1%.
3. The EAS data shows Max. rating. The test condition is V_{DD}=50V, V_{GS}=10V, L=1mH, I_{AS}=25A.
4. Pulse Test: Pulse Width≦300μs, Duty Cycle≦2%.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

CHARACTERISTIC CURVE

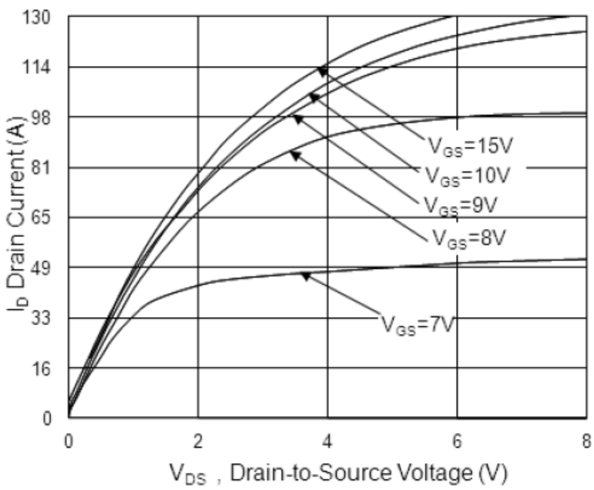


Fig.1 Typical Output Characteristics

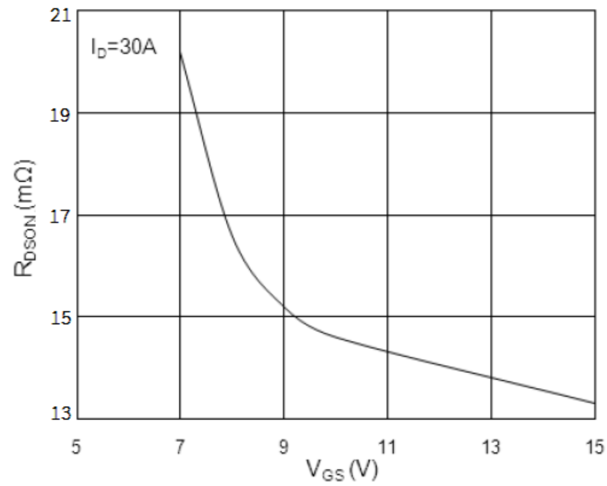


Fig.2 On-Resistance v.s Gate-Source

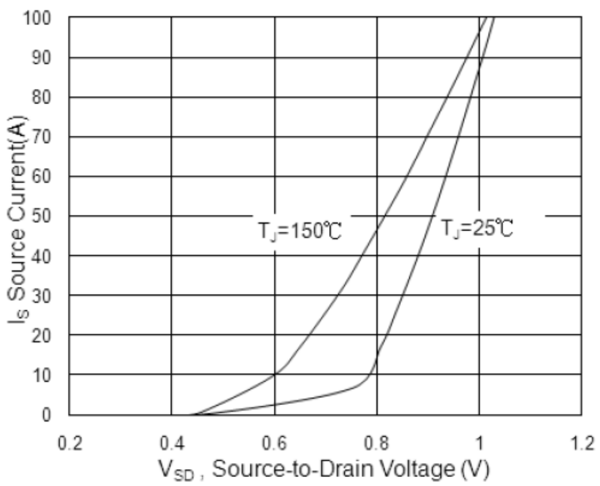


Fig.3 Forward Characteristics of Reverse

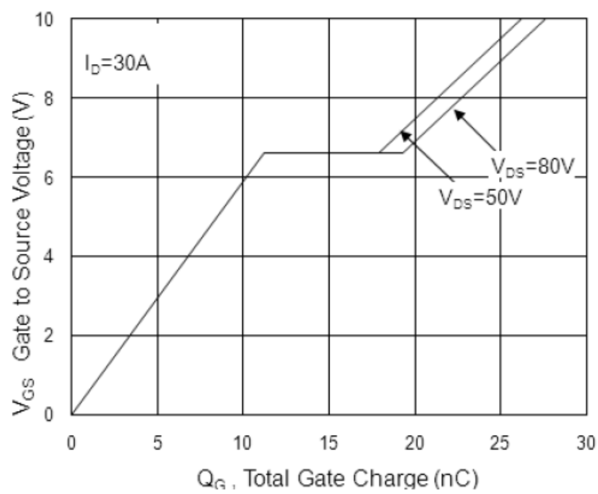


Fig.4 Gate-Charge Characteristics

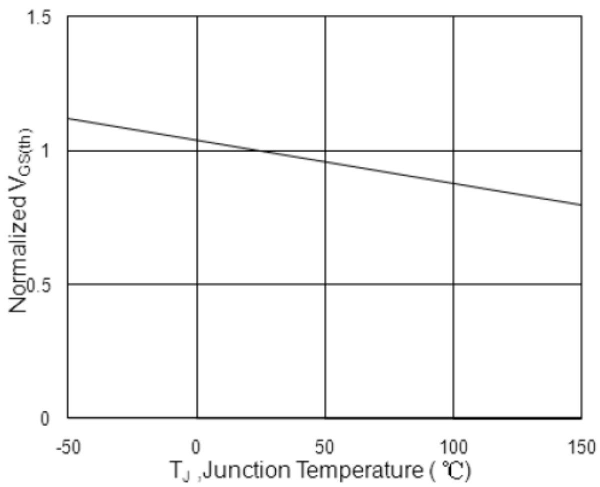


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

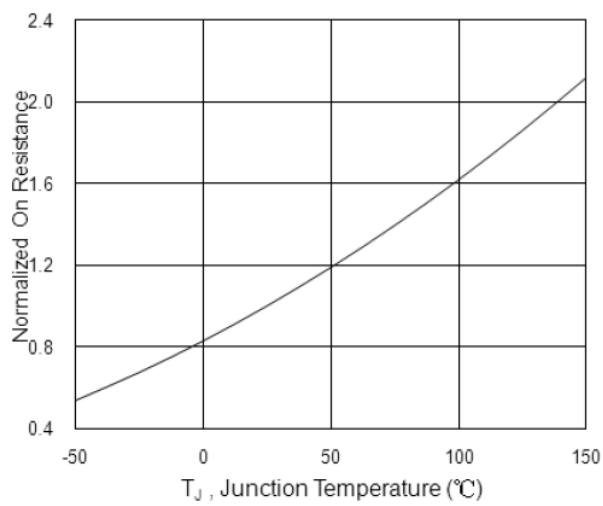


Fig.6 Normalized R_{DSON} vs. T_J

Elektronische Bauelemente

SSE50N10-C

54A, 100V, $R_{DS(ON)}$ 20mΩ

N-Ch Enhancement Mode Power MOSFET

CHARACTERISTIC CURVE

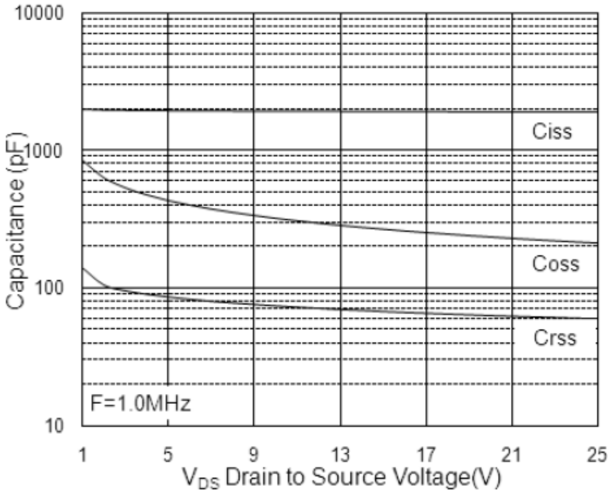


Fig.7 Capacitance

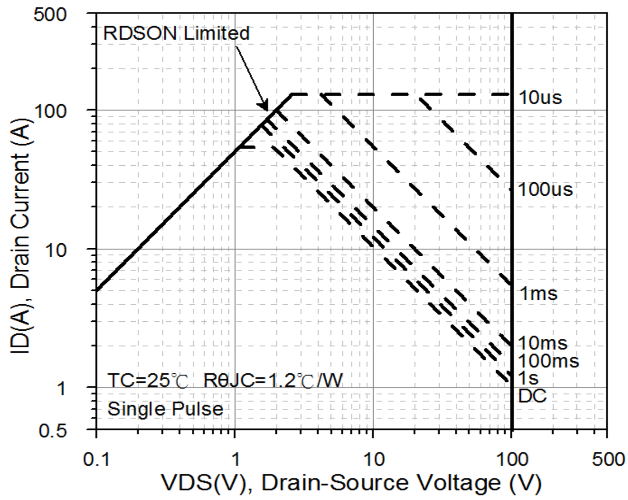


Fig.8 Safe Operating Area

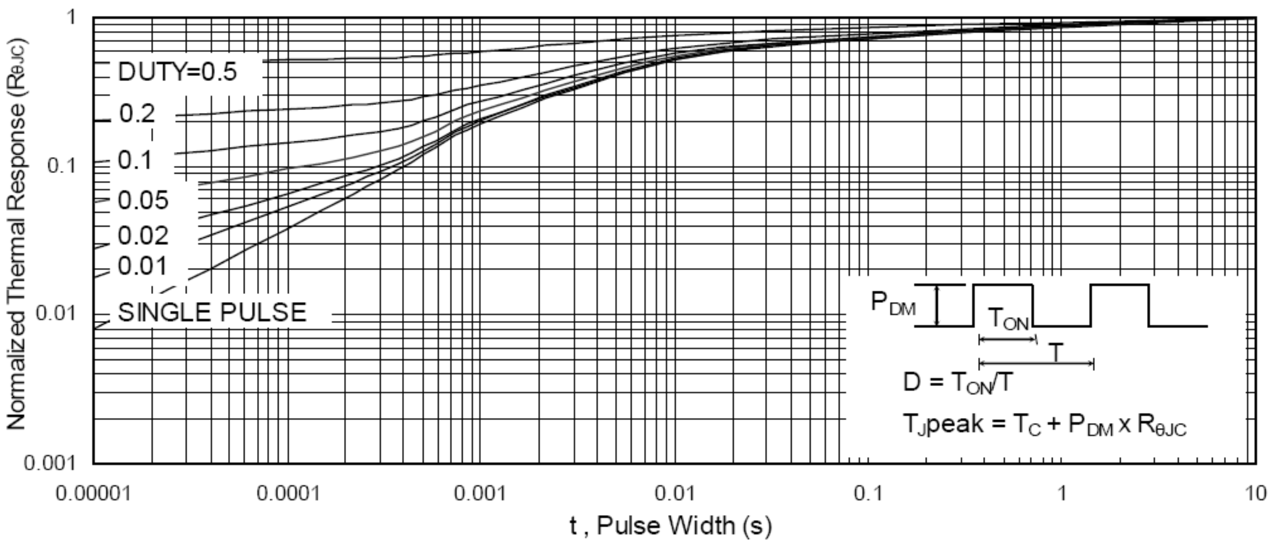


Fig.9 Normalized Maximum Transient Thermal Impedance

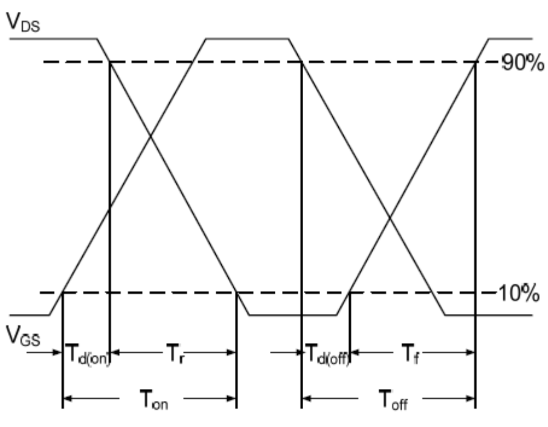


Fig.10 Switching Time Waveform

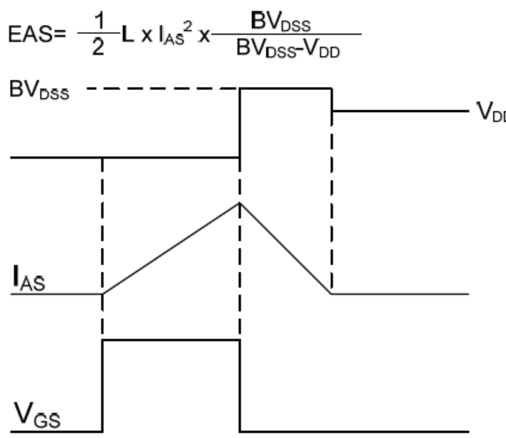


Fig.11 Unclamped Inductive Switching Wave