Elektronische Bauelemente

SSE68N10S-C

68A, 100V, $R_{DS(ON)}$ 9.8mΩ
N-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

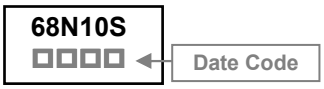
The SSE68N10S-C is the highest performance trench N-Ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSE68N10S-C meet the RoHS and Green Product requirement with full function reliability approved.

FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

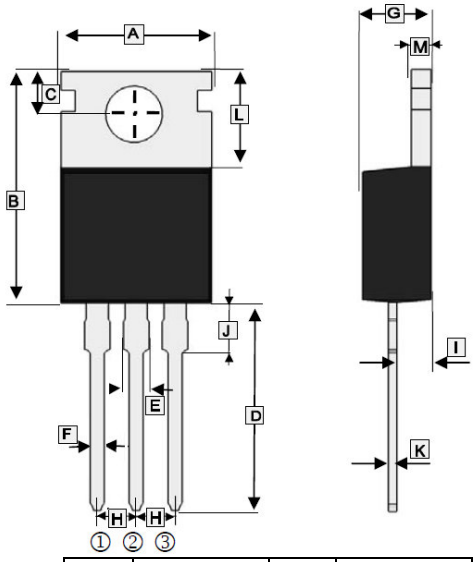
MARKING

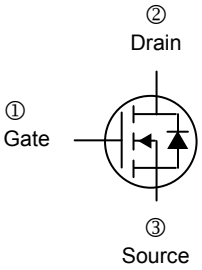


ORDER INFORMATION

Part Number	Type
SSE68N10S-C	Lead (Pb)-free and Halogen-free

TO-220





REF.	Millimeter Min.	Millimeter Max.	REF.	Millimeter Min.	Millimeter Max.
A	9.96	10.36	H	2.54 BSC.	
B	14.7	16	I	2.04	2.92
C	2.74 BSC.		J	3.745 REF.	
D	12.7	14.73	K	0.356	0.5
E	1.15	1.82	L	5.85	6.85
F	0.39	1.01	M	0.51	1.39
G	3.56	4.82			

ABSOLUTE MAXIMUM RATINGS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1] @V_{GS}=10V	T_C=25°C	I_D	68	A
	T_C=100°C		48	
Pulsed Drain Current [2]		I_{DM}	160	A
Power Dissipation	T_C=25°C	P_D	81	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	°C
Thermal Resistance Ratings				
Maximum Thermal Resistance Junction- Ambient [1]		$R_{\theta JA}$	50	°C/W
Maximum Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	1.55	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0V, I_D=250μA
Gate Threshold Voltage	$V_{GS(th)}$	1.4	-	2.4	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transconductance	g_{fs}	-	80	-	S	V_{DS}=5V, I_D=10A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	V_{DS}=80V, V_{GS}=0V, T_J=25°C
				100		V_{DS}=80V, V_{GS}=0V, T_J=100°C
Static Drain-Source On-Resistance [3]	$R_{DS(ON)}$	-	8.4	9.8	mΩ	V_{GS}=10V, I_D=20A
		-	11.3	13		V_{GS}=4.5V, I_D=20A
Gate Resistance	R_g	-	1.4	-	Ω	V_{DS}=V_{GS}=0V, f=1MHz
Total Gate Charge (4.5V)	Q_g	-	12	-	nC	I_D=20A V_{DD}=50V V_{GS}=10V
Total Gate Charge	Q_g	-	24	-		
Gate-Source Charge	Q_{gs}	-	4	-		
Gate-Drain Change	Q_{gd}	-	6	-		
Turn-on Delay Time	$T_{d(on)}$	-	6	-	nS	V_{DD}=50V I_D=20A V_{GS}=10V R_G=10Ω
Rise Time	T_r	-	4	-		
Turn-off Delay Time	$T_{d(off)}$	-	18	-		
Fall Time	T_f	-	3	-		
Input Capacitance	C_{iss}	-	1450	-	pF	V_{GS}=0V V_{DS}=50V f=1MHz
Output Capacitance	C_{oss}	-	273	-		
Reverse Transfer Capacitance	C_{rss}	-	5	-		
Source-Drain Diode						
Diode Forward Voltage [3]	V_{SD}	-	-	1.2	V	I_F=20A, V_{GS}=0V
Reverse Recovery Time	t_{rr}	-	40	-	nS	V_R=50V, I_F=20A , dI_F/dt=500A/μs
Reverse Recovery Charge	Q_{rr}	-	152	-	nC	

Notes:
1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The Pulse width limited by maximum junction temperature, Pulse Width ≤10μs, Duty Cycle≤2%.
3. The Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%.

TYPICAL CHARACTERISTIC

Fig 1. Typical Output Characteristics

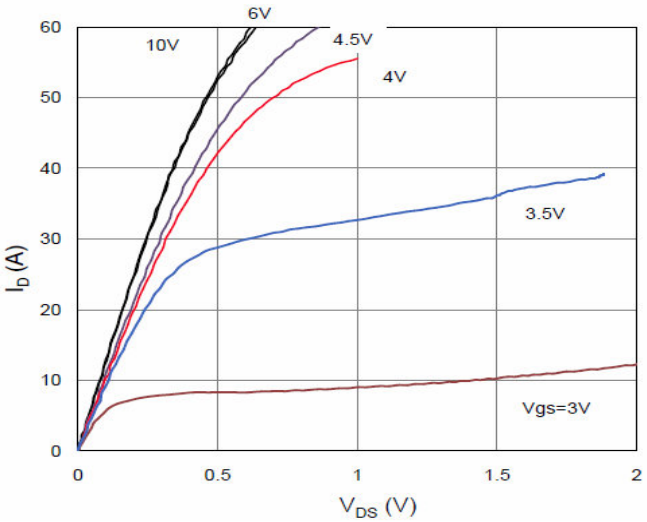


Figure 2. On-Resistance vs. Gate-Source Voltage

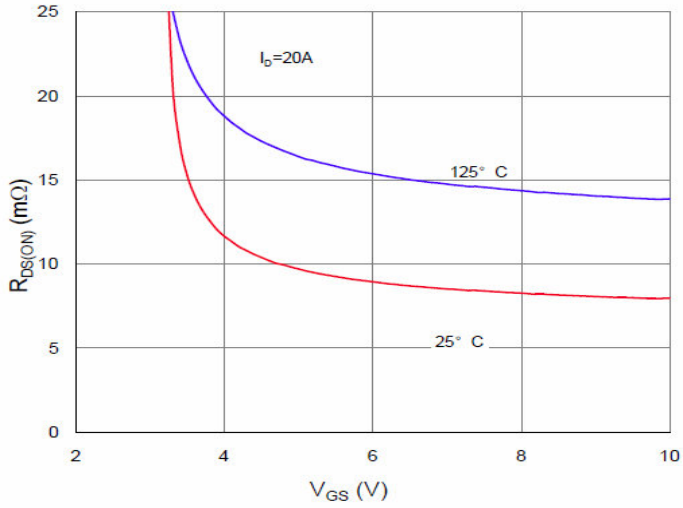


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

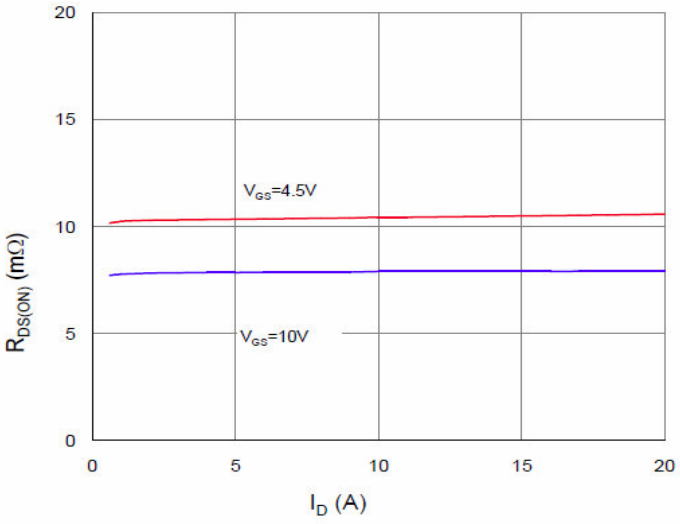


Figure 4. Normalized On-Resistance vs. Junction Temperature

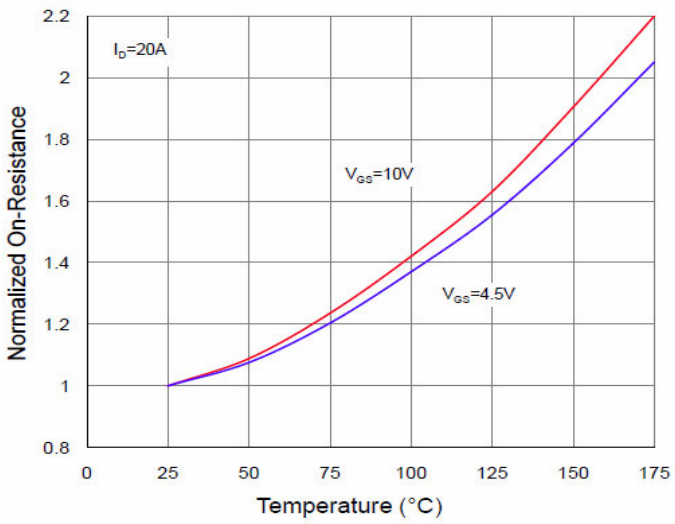


Figure 5. Typical Transfer Characteristics

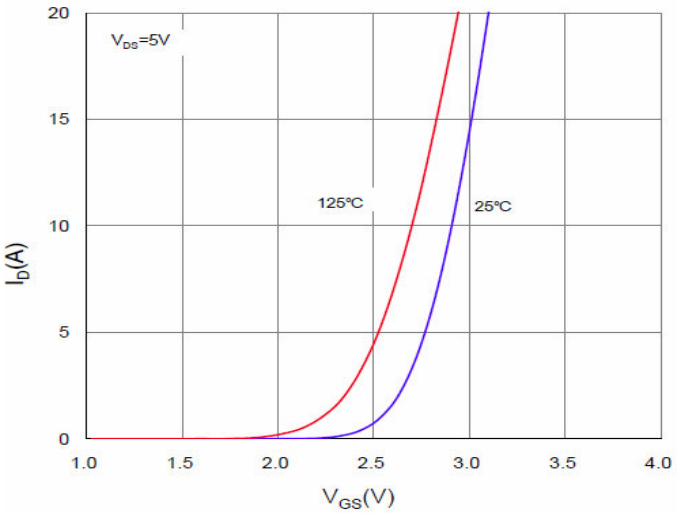
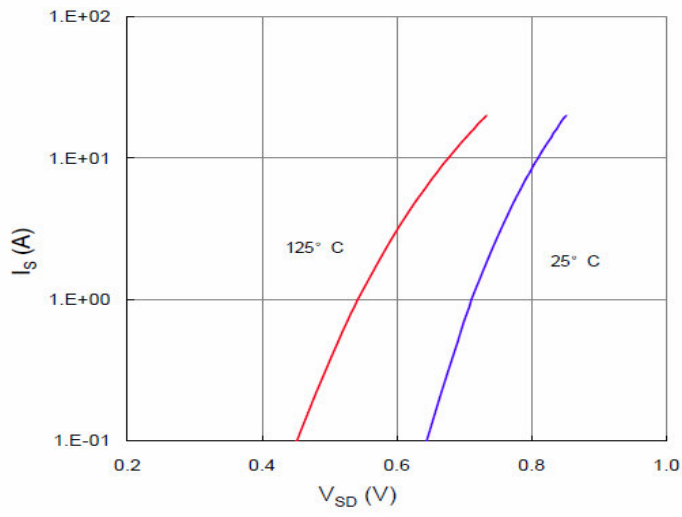


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTIC

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

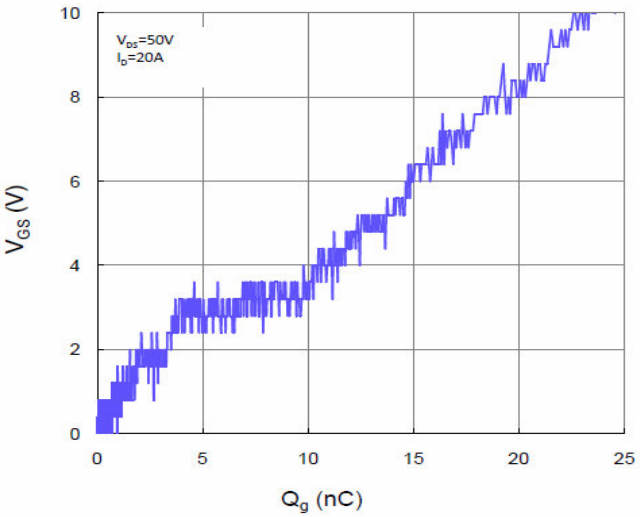


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

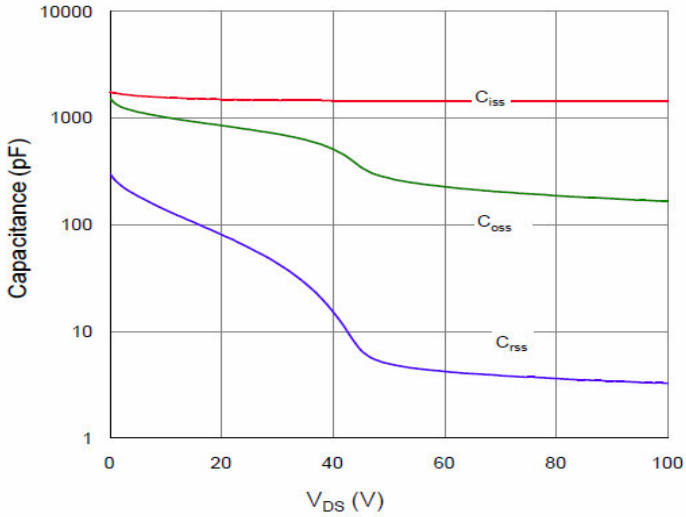


Figure 9. Maximum Safe Operating Area

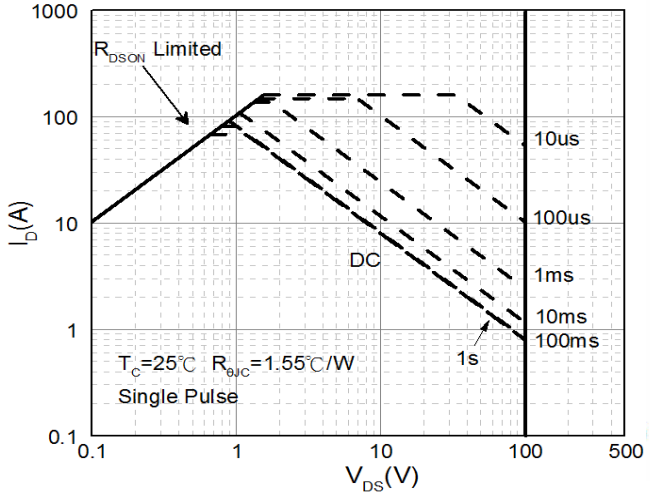


Figure 10. Maximun Drain Current vs. Case Temperature

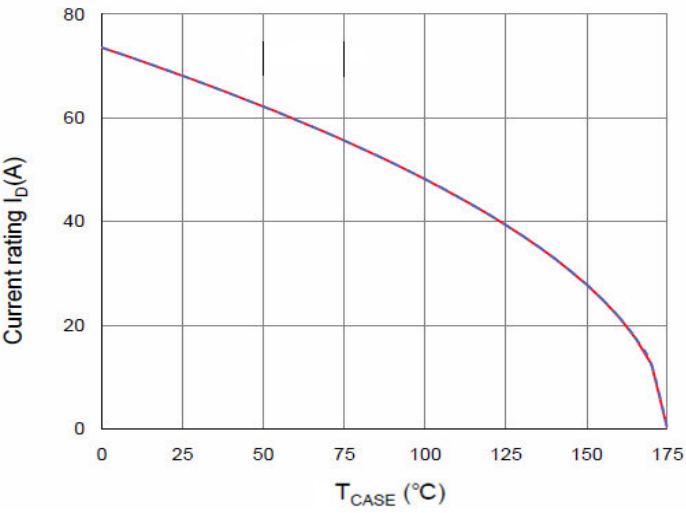


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case