Elektronische Bauelemente

SID25N10-C

25A, 100V, $R_{DS(ON)}$ 48mΩ

N-Ch Enhancement Mode Power MOSFET

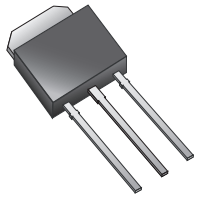
RoHS Compliant Product
A suffix of "-C" specifies halogen free

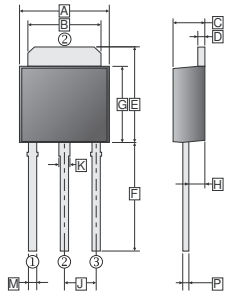
DESCRIPTION

The SID25N10-C is the highest performance trench N-Ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SID25N10-C meet the RoHS and Green Product requirement with full function reliability approved.

TO-251



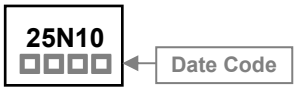


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	G	5.40	6.25
B	4.90	5.50	H	0.85	1.50
C	2.15	2.40	J	2.30 Typ.	
D	0.43	0.90	K	0.60	1.05
E	6.50	7.50	M	0.50	0.90
F	7.20	9.65	P	0.43	0.62

FEATURES

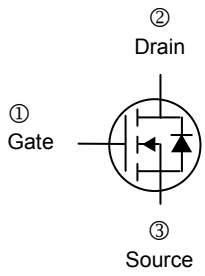
- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING



ORDER INFORMATION

Part Number	Type
SID25N10-C	Lead (Pb)-free and Halogen-free



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current @V_{GS}=10V [1]	T_C=25°C	I_D	25	A
	T_C=100°C		15	A
Pulsed Drain Current [3]		I_{DM}	45	A
Total Power Dissipation	T_C=25°C	P_D	52	W
	T_A=25°C		2	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	°C
Thermal Resistance Ratings				
Maximum Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	62.5	°C/W
Maximum Thermal Resistance Junction-Ambient [2]			110	
Maximum Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	2.4	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	100	-	-	V	V_{GS}=0, I_D=250μA
Gate-Threshold Voltage		$V_{GS(th)}$	1	-	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	1	μA	V_{DS}=80V, V_{GS}=0
	T_J=55°C		-	-	100		V_{DS}=80V, V_{GS}=0
Static Drain-Source On-Resistance [4]		$R_{DS(ON)}$	-	43	48	mΩ	V_{GS}=10V, I_D=25A
			-	45	50		V_{GS}=4.5V, I_D=15A
Total Gate Charge		Q_g	-	59	-	nC	I_D=20A V_{DS}=80V V_{GS}=10V
Gate-Source Charge		Q_{gs}	-	9.7	-		
Gate-Drain Change		Q_{gd}	-	11.8	-		
Turn-on Delay Time [2]		$T_{d(on)}$	-	10.4	-	nS	V_{DD}=50V I_D=20A V_{GS}=10V R_G=3.3Ω
Rise Time		T_r	-	46	-		
Turn-off Delay Time		$T_{d(off)}$	-	54	-		
Fall Time		T_f	-	10	-		
Input Capacitance		C_{iss}	-	3848	-	pF	V_{GS}=0 V_{DS}=15V f=1MHz
Output Capacitance		C_{oss}	-	137	-		
Reverse Transfer Capacitance		C_{rss}	-	82	-		
Gate Resistance		R_g	-	1.6	4	Ω	f=1MHz
Source-Drain Diode							
Continuous Source Current [1]		I_S	-	-	25	A	
Pulsed Source Current [3]		I_{SM}	-	-	45	A	
Diode Forward Voltage [4]		V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0, T_J=25°C
Reverse Recovery Time		T_{rr}	-	30	-	nS	I_F=20A, dI/dt=100A/μs T_J=25°C
Reverse Recovery Charge		Q_{rr}	-	37	-	nC	

Notes:
1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. When mounted on minimum pad of 2 oz. copper.
3. Pulse width limited by maximum junction temperature.
4. The data tested by pulsed, pulse width≦300μs, duty cycle≦2%.

CHARACTERISTIC CURVES

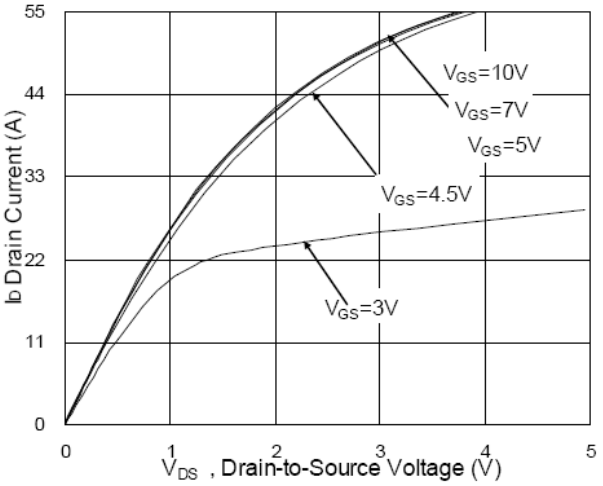


Fig.1 Typical Output Characteristics

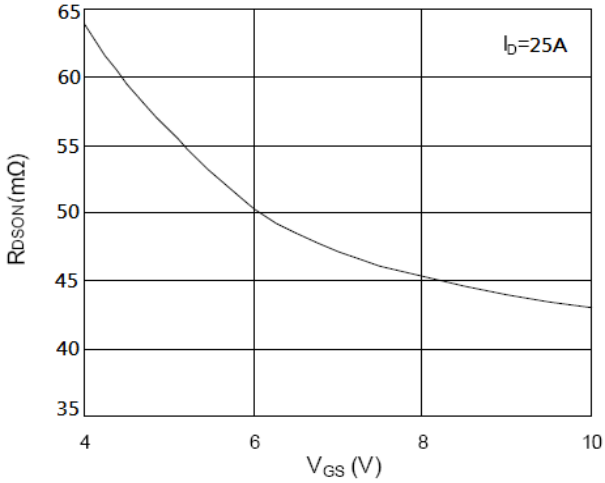


Fig.2 On-Resistance vs. Gate-Source

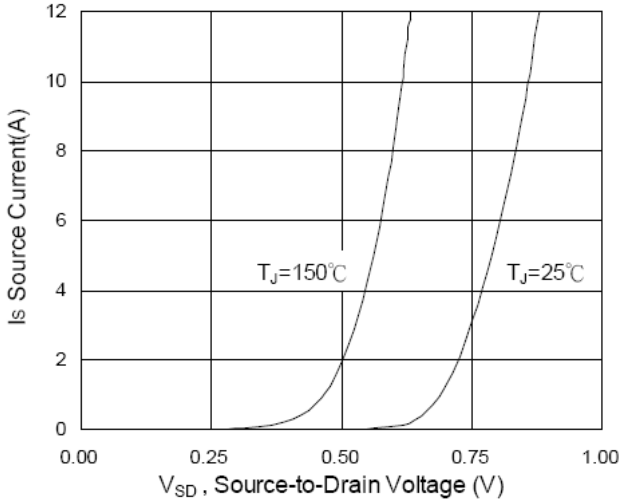


Fig.3 Forward Characteristics Of Reverse

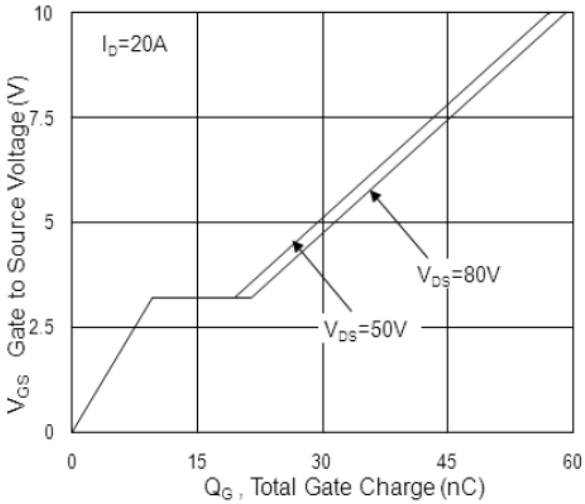


Fig.4 Gate-Charge Characteristics

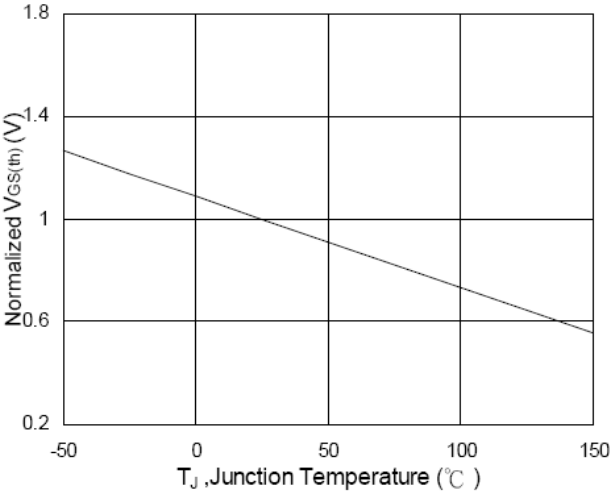


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

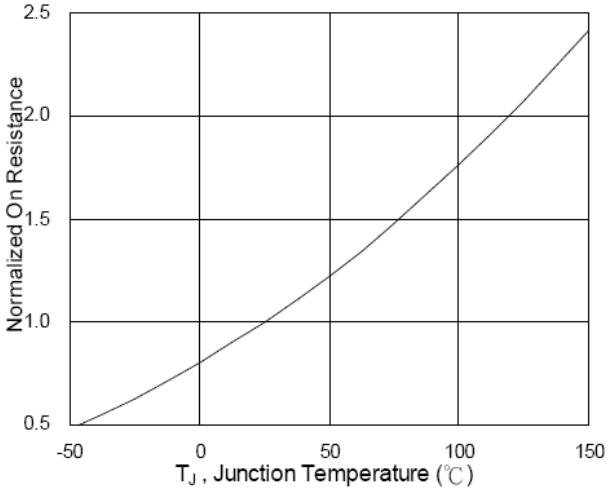


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVES

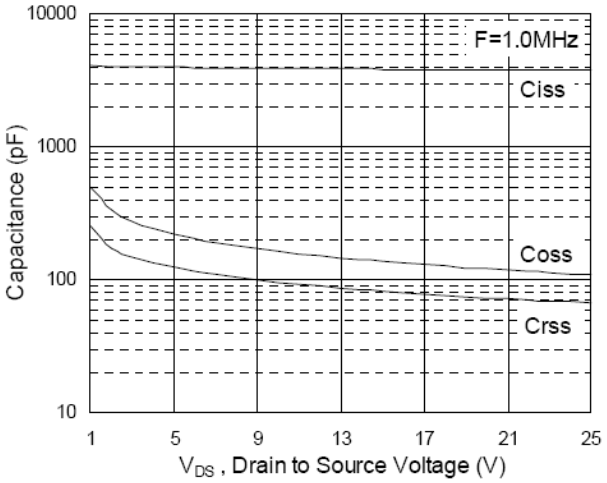


Fig.7 Capacitance

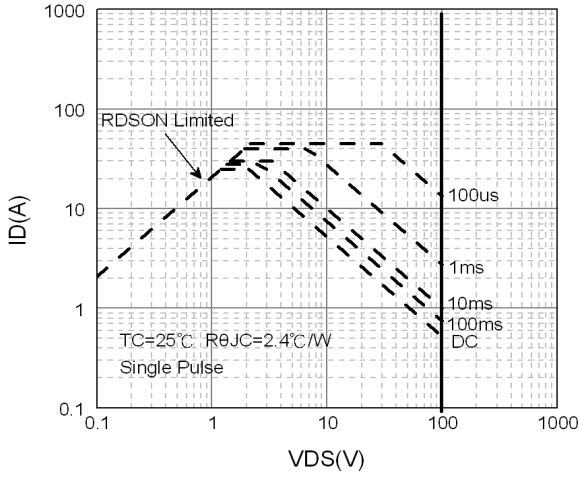


Fig.8 Safe Operating Area

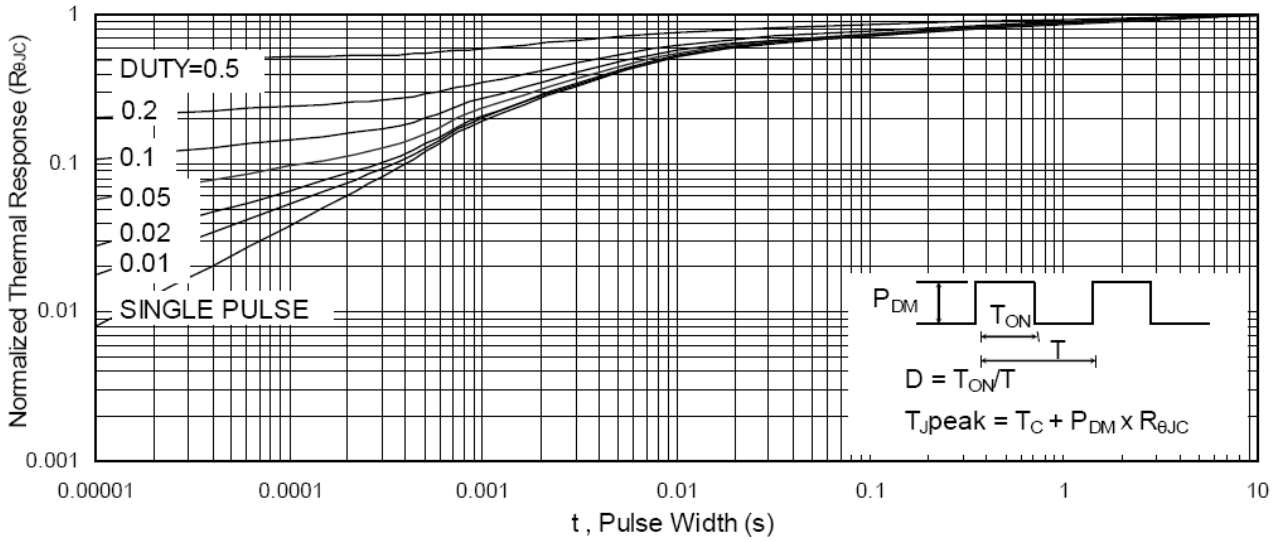


Fig.9 Normalized Maximum Transient Thermal Impedance

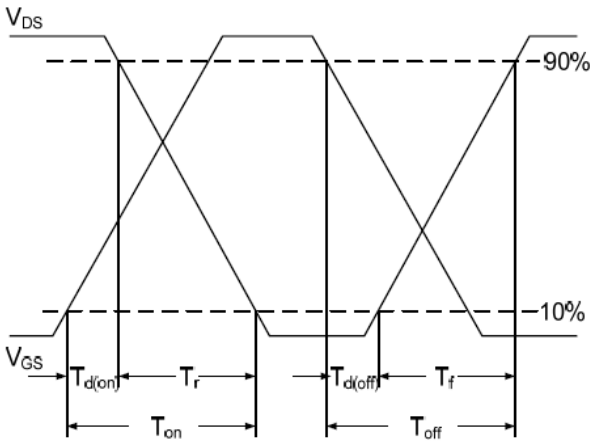


Fig.10 Switching Time Waveform

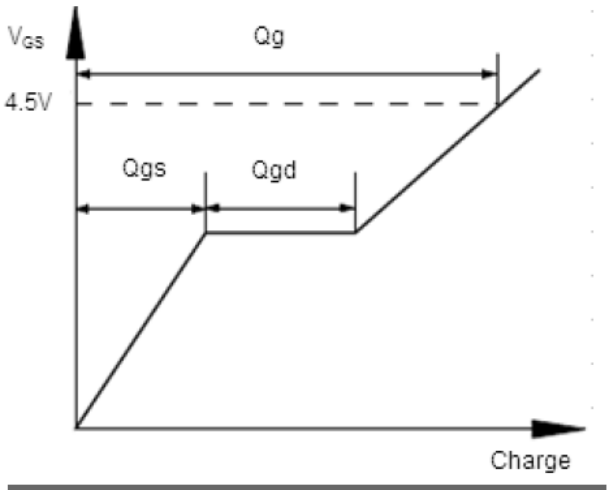


Fig.11 Gate Charge Waveform