Elektronische Bauelemente

SSD07N65H-C

7.3A, 650V, $R_{DS(ON)}$ 0.65Ω
N-Channel Super Junction Power MOSFET

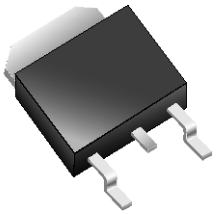
RoHS Compliant Product
A suffix of "-C" specifies halogen free

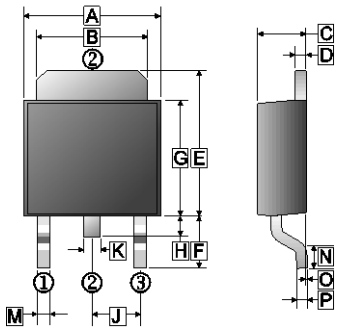
DESCRIPTION

The SSD07N65H-C is power MOSFET using Super Junction Technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of low EMI to designers as well as low switching loss, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSD07N65H-C meet the RoHS and Green Product requirement with full function reliability approved.

TO-252(D-Pack)





REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.3	6.9	J	2.3 REF.	
B	4.95	5.53	K	0.89 REF.	
C	2.1	2.5	M	0.45	1.14
D	0.4	0.9	N	1.55 Typ.	
E	6	7.7	O	0	0.15
F	2.90 REF		P	0.58 REF.	
G	5.4	6.4			
H	0.6	1.2			

FEATURES

- Advanced Super Junction Technology
- Super Low Gate Charge
- Green Device Available

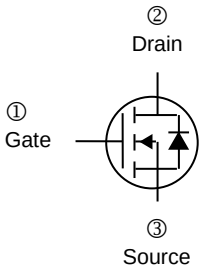
MARKING

PACKAGE INFORMATION

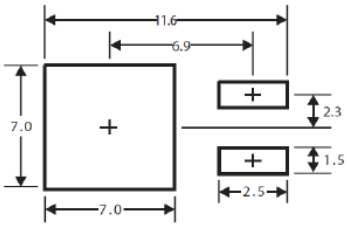
Package	MPQ	Leader Size
TO-252	2.5K	13 inch

ORDER INFORMATION

Part Number	Type
SSD07N65H-C	Lead (Pb)-free and Halogen-free



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current [1,5] @V_{GS}=10V	T_C=25°C	I_D	7.3	A
	T_C=100°C		4.6	
Pulsed Drain Current [3]		I_{DM}	22	A
Total Power Dissipation	T_C=25°C	P_D	52	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	°C
Thermal Resistance Ratings				
Maximum Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	62.5	°C/W
Maximum Thermal Resistance Junction-Ambient [2]			110	
Maximum Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	2.4	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	650	-	-	V	V_{GS}=0, I_D=250μA
Gate Threshold Voltage		$V_{GS(th)}$	2	-	4	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}=±30V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	1	μA	V_{DS}=520V, V_{GS}=0
	T_J=55°C		-	-	5		V_{DS}=520V, V_{GS}=0
Static Drain-Source On-Resistance [4]		$R_{DS(ON)}$	-	0.58	0.65	Ω	V_{GS}=10V, I_D=2.1A
Total Gate Charge		Q_g	-	13.8	-	nC	I_D=7.3A V_{DS}=520V V_{GS}=10V
Gate-Source Charge		Q_{gs}	-	3.6	-		
Gate-Drain Change		Q_{gd}	-	5.6	-		
Turn-on Delay Time		$T_{d(on)}$	-	18	-	nS	V_{DS}=325V I_D=7.3A V_{GS}=10V R_G=25Ω
Rise Time		T_r	-	33	-		
Turn-off Delay Time		$T_{d(off)}$	-	80	-		
Fall Time		T_f	-	28	-		
Input Capacitance		C_{iss}	-	545	-	pF	V_{GS}=0V V_{DS}=25V f=1MHz
Output Capacitance		C_{oss}	-	640	-		
Reverse Transfer Capacitance		C_{rss}	-	28.6	-		
Source-Drain Diode							
Diode Forward Voltage [4]		V_{SD}	-	-	1.4	V	V_{GS}=0, I_S=7.3A
Continuous Source Current [1,5]		I_S	-	-	7.3	A	
Pulsed Source Current [3]		I_{SM}	-	-	22	A	
Reverse Recovery Time		T_{rr}	-	272	-	nS	I_S=7.3A, dI/dt=100A/μs, V_{DD}=100V
Reverse Recovery Charge		Q_{rr}	-	3	-	μC	

Notes:
1. Surface Mounted on 1inch^2 FR-4 Board with 2oz copper.
2. When mounted on Min. copper pad.
3. Pulse Width limited by maximum junction temperature, pulse width≦ 10us, duty cycle≦ 2%.
4. The data tested by pulsed, Pulse Width≦ 300μs, Duty Cycle≦ 2%.
5. I_D limited by maximum junction temperature.

TYPICAL CHARACTERISTICS CURVE

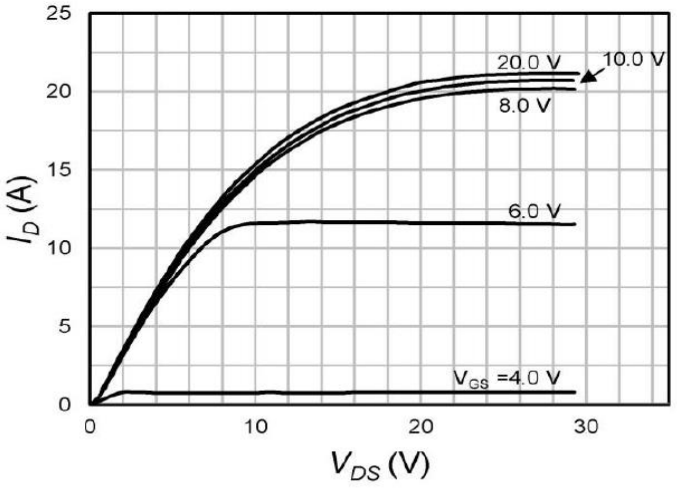


Fig.1 Typical Output Characteristics

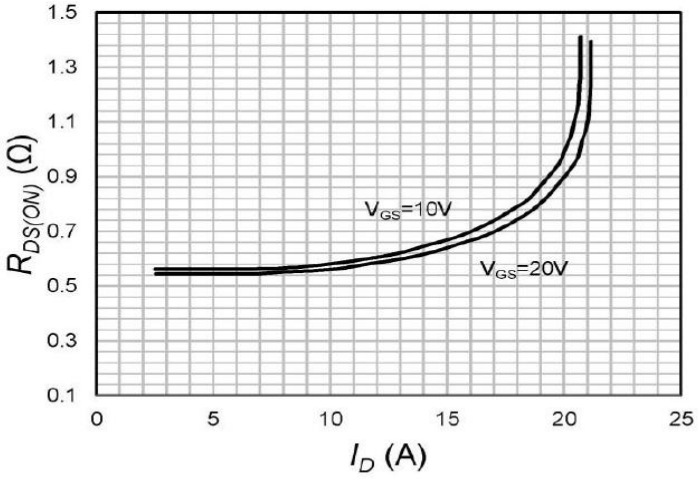


Fig.2 On-Resistance vs. Drain Current

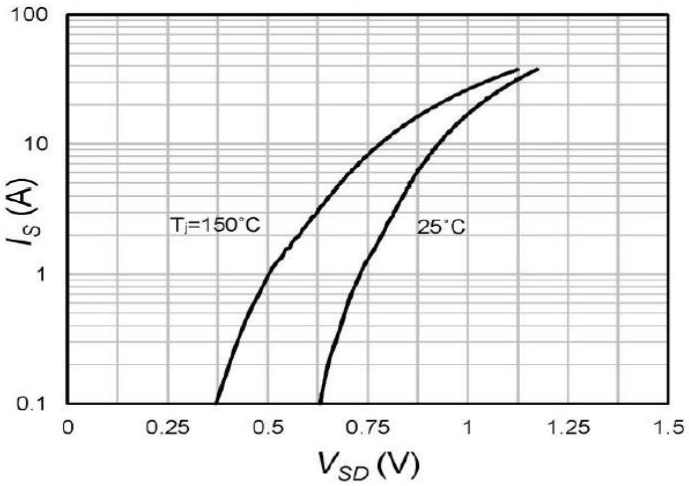


Fig.3 Forward Characteristics of Reverse

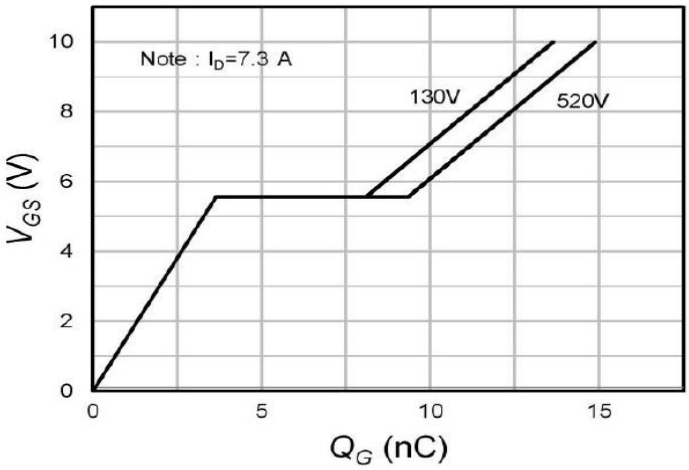


Fig.4 Gate-Charge Characteristics

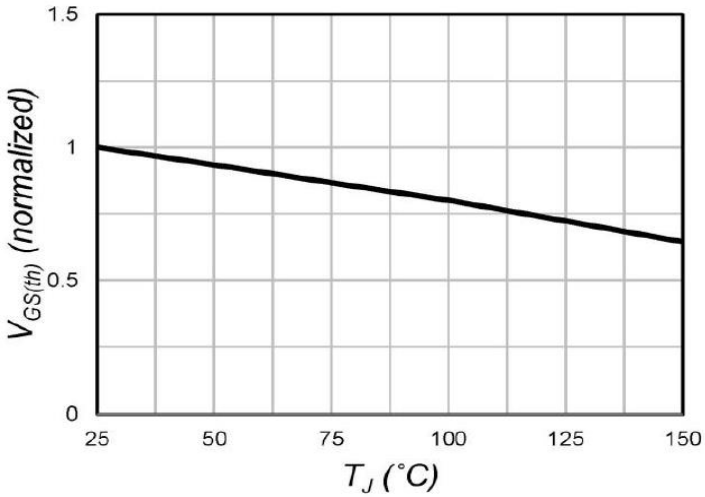


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

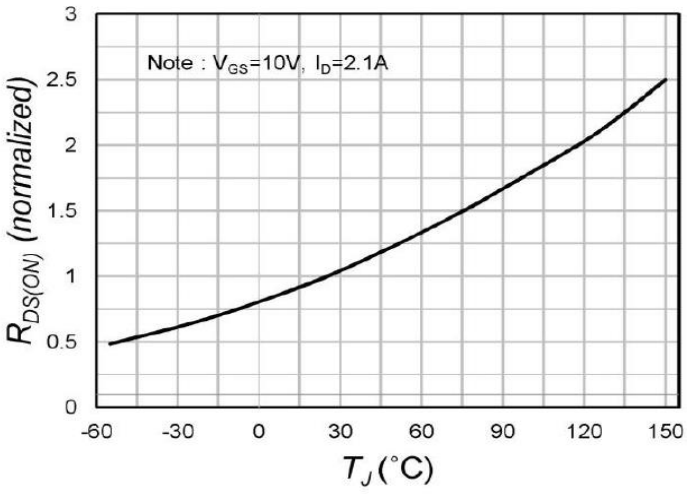


Fig.6 Normalized R_{DSON} vs. T_J

TYPICAL CHARACTERISTICS CURVE

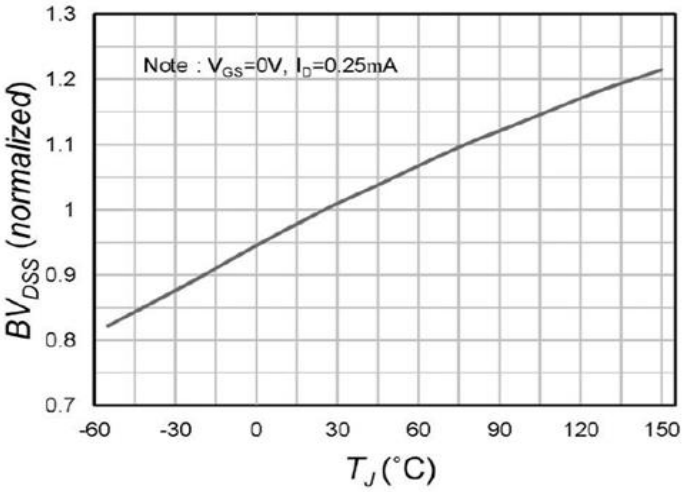


Fig.7 Drain-Source Breakdown Voltage(Normaized)

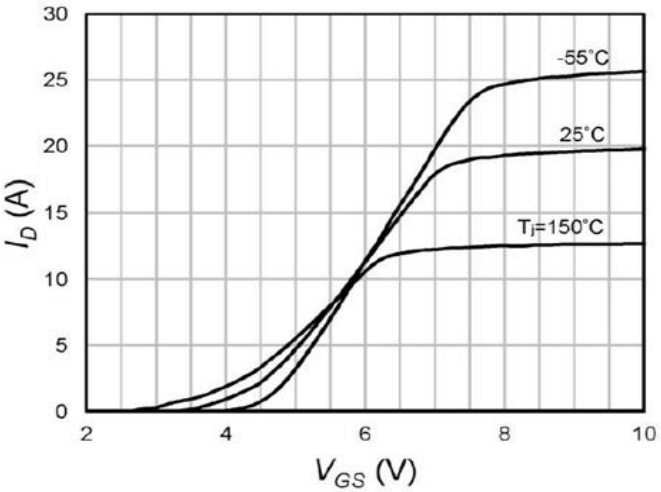


Fig.8 Transfer Characteristics

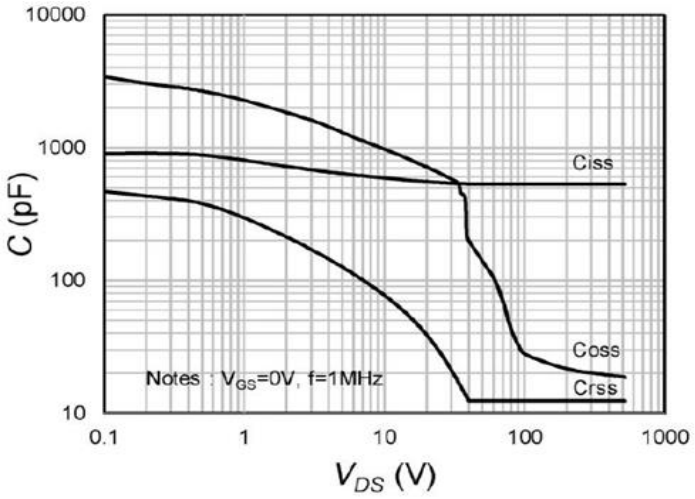


Fig.9 Capacitances

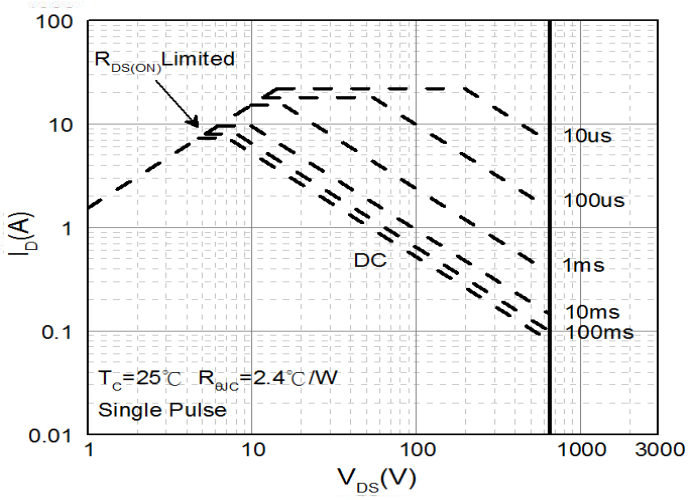


Fig.10 Safe Operating Area

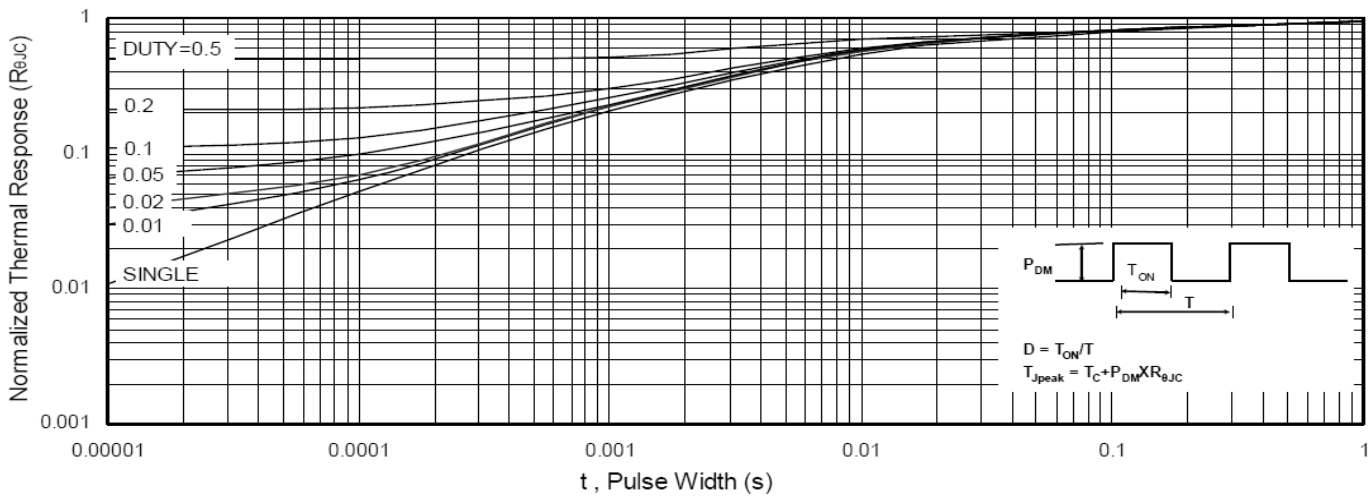


Fig.11 Normalized Maximum Transient Thermal Impedance