Elektronische Bauelemente

SSD15N10-C

15A, 100V, $R_{DS(ON)}$ 110mΩ
N-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSD15N10-C is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent R_{DSON} and gate charge for most of the synchronous buck converter applications.

The SSD15N10-C meet the RoHS and Green Product requirement with full function reliability approved.

FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING

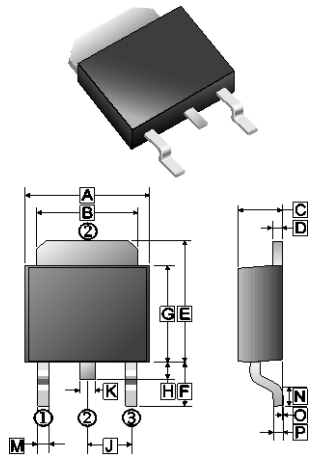
PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

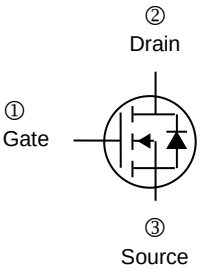
ORDER INFORMATION

Part Number	Type
SSD15N10-C	Lead (Pb)-free and Halogen-free

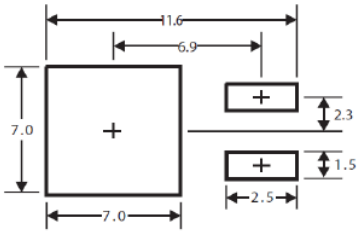
TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.30	6.90	J	2.30 REF.	
B	4.95	5.53	K	0.89 REF.	
C	2.10	2.50	M	0.45	1.14
D	0.40	0.90	N	1.55 TYP.	
E	6.00	7.70	O	0	0.15
F	2.90 REF.		P	0.58 REF.	
G	5.40	6.40			
H	0.60	1.20			



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current @V_{GS}=10V [1]	T_C=25°C	I_D	15	A
	T_C=100°C		10.5	A
Pulsed Drain Current [3]		I_{DM}	30	A
Power Dissipation	T_C=25°C	P_D	44.6	W
	T_A=25°C		2	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 ~ 150	°C
Thermal Resistance Ratings				
Maximum Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	62.5	°C/W
Maximum Thermal Resistance Junction-Ambient [2]			110	
Maximum Thermal Resistance Junction-Case		$R_{\theta JC}$	2.8	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Drain-Source Breakdown Voltage		BV_{DSS}	100	-	-	V	V_{GS}=0, I_D=250μA
Gate Threshold Voltage		$V_{GS(th)}$	1.0	-	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	1	μA	V_{DS}=80V, V_{GS}=0
	T_J=55°C		-	-	5		
Static Drain-Source On-Resistance [4]		$R_{DS(ON)}$	-	-	110	mΩ	V_{GS}=10V, I_D=8A
			-	-	120		V_{GS}=4.5V, I_D=6A
Total Gate Charge [2]		Q_g	-	26.2	-	nC	I_D=10A V_{DS}=80V V_{GS}=10V
Gate-Source Charge		Q_{gs}	-	4.6	-		
Gate-Drain (“Miller”) Change		Q_{gd}	-	5.1	-		
Turn-on Delay Time [2]		$T_{d(on)}$	-	4.2	-	nS	V_{DS}=50V I_D=10A V_{GS}=10V R_G=3.3Ω
Rise Time		T_r	-	8.2	-		
Turn-off Delay Time		$T_{d(off)}$	-	35.6	-		
Fall Time		T_f	-	9.6	-		
Input Capacitance		C_{iss}	-	1535	-	pF	V_{GS}=0 V_{DS}=15V f=1MHz
Output Capacitance		C_{oss}	-	60	-		
Reverse Transfer Capacitance		C_{rss}	-	37	-		
Gate Resistance		R_g	-	2	-	Ω	f=1MHz
Source-Drain Diode							
Continuous Source Current [1]		I_S	-	-	15	A	
Pulsed Source Current [3],		I_{SM}	-	-	30		
Forward On Voltage [2]		V_{SD}	-	-	1.2	V	V_{GS}=0V, I_S=8A, T_J=25°C
Reverse Recovery Time		t_{rr}	-	37	-	nS	I_F=10A, dI/dt=100A/μs, T_J=25°C
Reverse Recovery Charge		Q_{rr}	-	27.3	-	nC	

Notes:
1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. When mounted on minimum pad of copper.
3. The power dissipation is limited by 150°C junction temperature.
4. The data tested by pulsed, pulse width≦ 300us, duty cycle≦ 2%.

CHARACTERISTICS CURVE

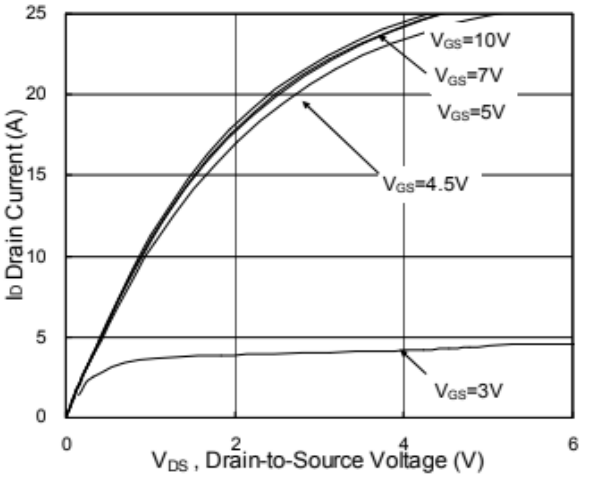


Fig.1 Typical Output Characteristics

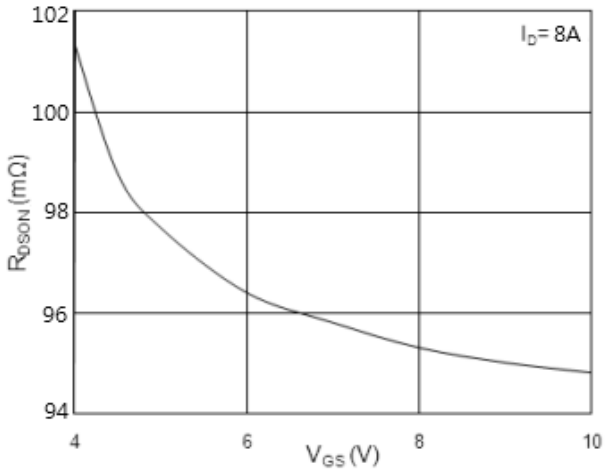


Fig.2 On-Resistance vs. Gate-Source

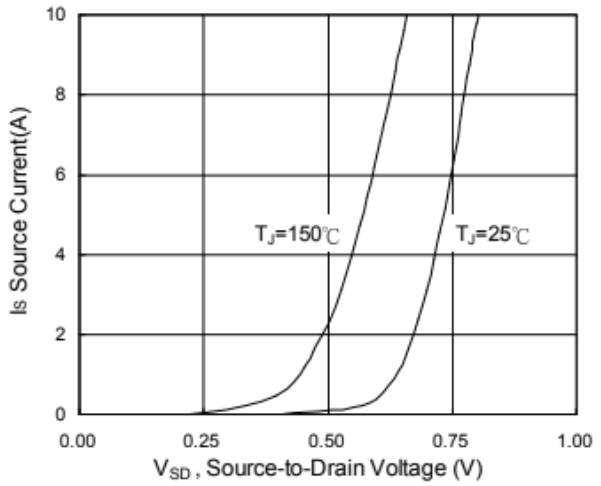


Fig.3 Forward Characteristics Of Reverse

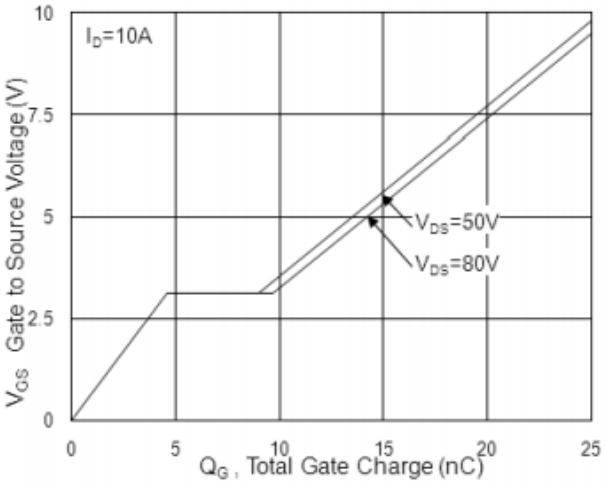


Fig.4 Gate-Charge Characteristics

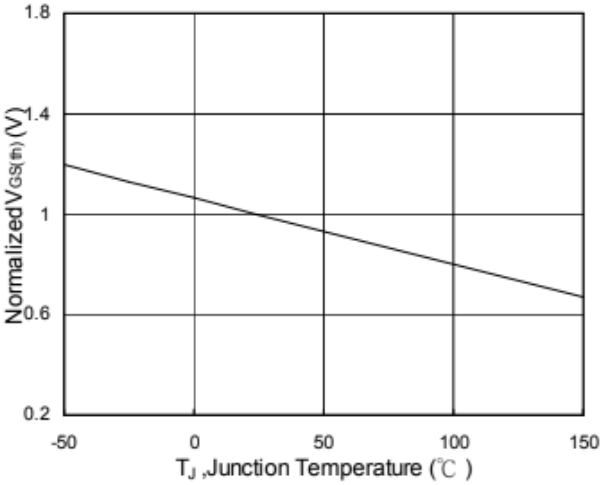


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

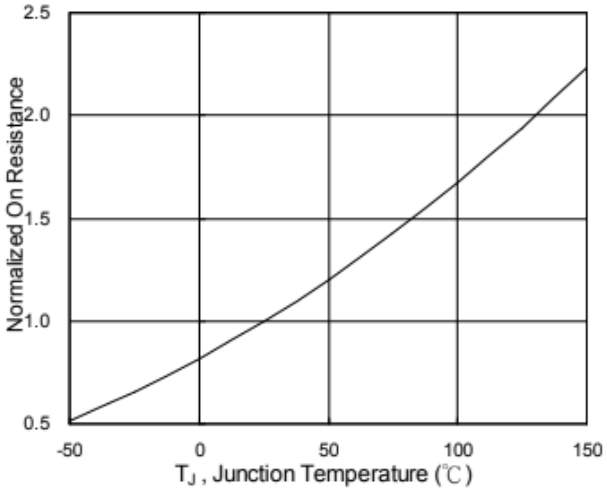


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTICS CURVE

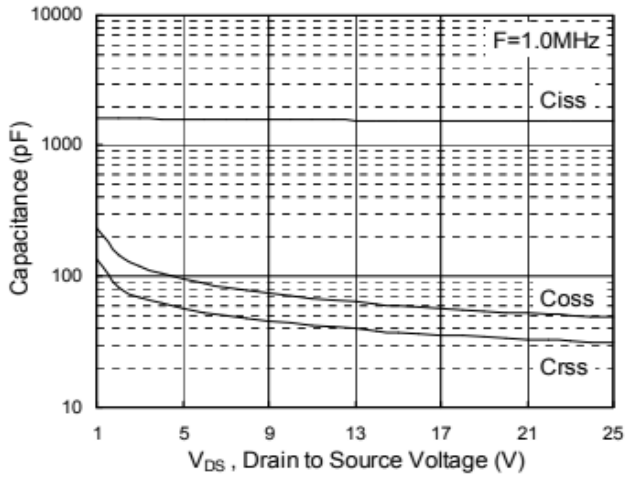


Fig.7 Capacitance

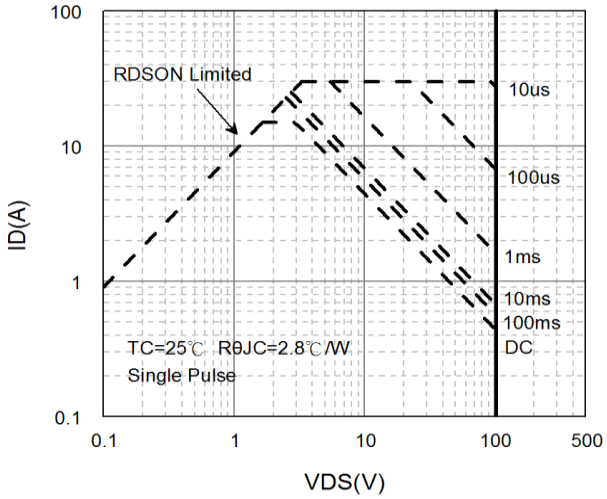


Fig.8 Safe Operating Area

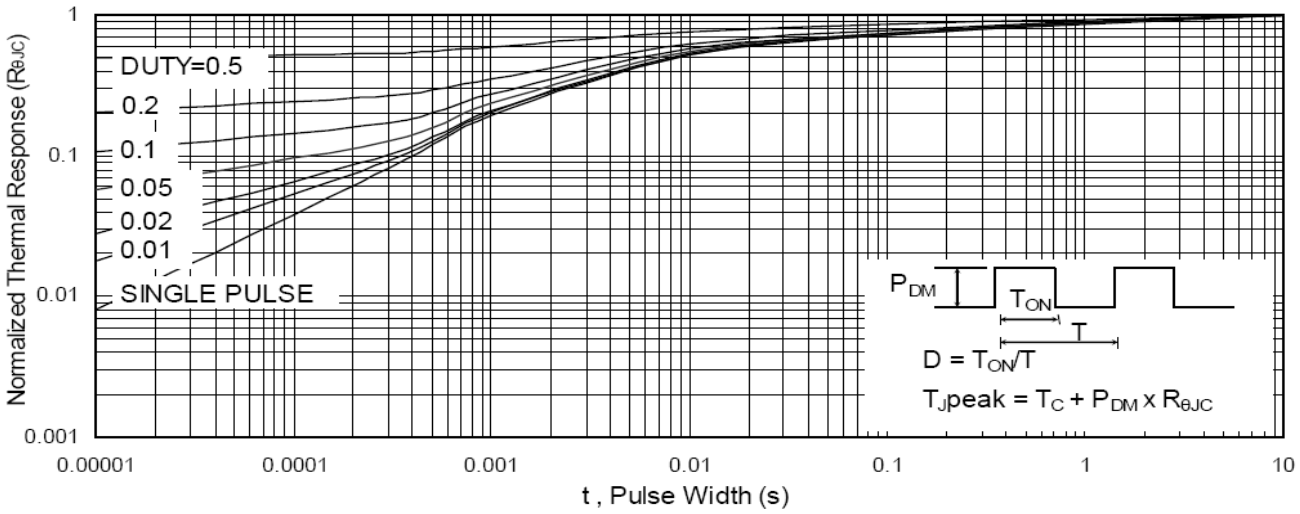


Fig.9 Normalized Maximum Transient Thermal Impedance

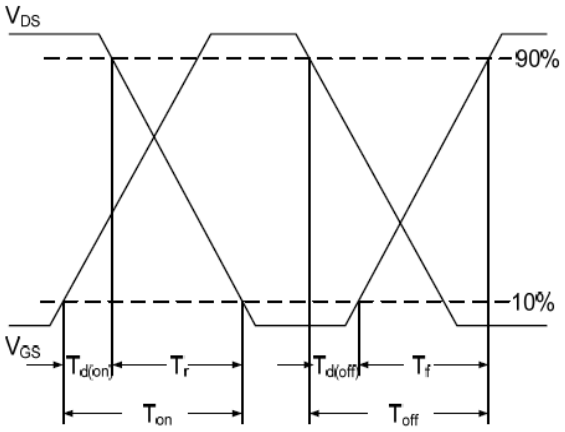


Fig.10 Switching Time Waveform

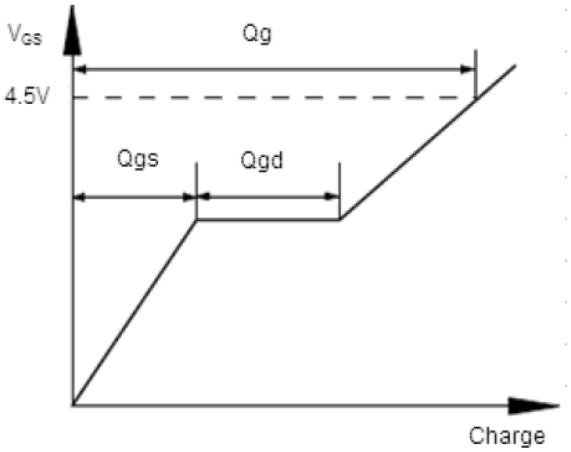


Fig.11 Gate Charge Waveform