

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSD29N10J-C is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications.

The SSD29N10J-C meet the RoHS and Green Product requirement with full function reliability approved.

FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Green Device Available

MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

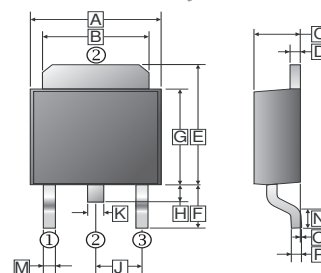
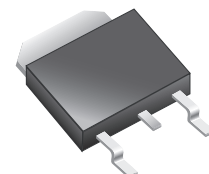
ORDER INFORMATION

Part Number	Type
SSD29N10J-C	Lead (Pb)-free and Halogen-free

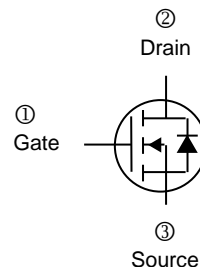
ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current @ $V_{GS}=10\text{V}$ ¹	I_D	$T_C=25^{\circ}\text{C}$	29
		$T_C=100^{\circ}\text{C}$	18.5
Pulsed Drain Current ⁴	I_{DM}	45	A
Total Power Dissipation ³	P_D	$T_C=25^{\circ}\text{C}$	52
		$T_A=25^{\circ}\text{C}$	2
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^{\circ}\text{C}$
Thermal Resistance Rating			
Maximum Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	62.5	$^{\circ}\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Ambient ²		110	$^{\circ}\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	2.4	$^{\circ}\text{C} / \text{W}$

TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.9	J	2.3 REF.	
B	4.95	5.53	K	0.89 REF.	
C	2.1	2.5	M	0.45	1.14
D	0.41	0.9	N	1.55 Typ.	
E	6	7.5	O	0	0.13
F	2.90 REF.		P	0.58 REF.	
G	5.4	6.4			
H	0.6	1.2			



ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Drain-Source Breakdown Voltage	BV_{DSS}	100	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$	
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{V}$	
Drain-Source Leakage Current	I_{DSS}	$T_J=25^\circ\text{C}$	-	-	1	μA	$V_{DS}=80\text{V}, V_{GS}=0$
		$T_J=55^\circ\text{C}$	-	-	100		$V_{DS}=80\text{V}, V_{GS}=0$
Static Drain-Source On-Resistance ⁴	$R_{DS(ON)}$	-	43	48	m Ω	$V_{GS}=10\text{V}, I_D=25\text{A}$	
		-	45	50		$V_{GS}=4.5\text{V}, I_D=15\text{A}$	
Total Gate Charge	Q_g	-	59	-	nC	$I_D=20\text{A}$ $V_{DS}=80\text{V}$ $V_{GS}=10\text{V}$	
Gate-Source Charge	Q_{gs}	-	9.7	-			
Gate-Drain Change	Q_{gd}	-	11.8	-			
Turn-on Delay Time	$T_{d(on)}$	-	10.4	-	nS	$V_{DD}=50\text{V}$ $I_D=20\text{A}$ $V_{GS}=10\text{V}$ $R_G=3.3\Omega$	
Rise Time	T_r	-	46	-			
Turn-off Delay Time	$T_{d(off)}$	-	54	-			
Fall Time	T_f	-	10	-			
Input Capacitance	C_{iss}	-	3848	-	pF	$V_{GS}=0$ $V_{DS}=15\text{V}$ $f=10\text{MHz}$	
Output Capacitance	C_{oss}	-	137	-			
Reverse Transfer Capacitance	C_{rss}	-	82	-			
Gate Resistance	R_g	-	1.6	4	Ω	$f=1\text{MHz}$	
Source-Drain Diode							
Continuous Source Current ¹	I_S	-	-	29	A	$V_D=V_G=0, \text{Force Current}$	
Pulsed Source Current ⁴	I_{SM}	-	-	45	A		
Diode Forward Voltage ⁴	V_{SD}	-	-	1.2	V	$I_S=1\text{A}, V_{GS}=0, T_J=25^\circ\text{C}$	
Reverse Recovery Time	T_{rr}	-	30	-	nS	$I_F=20\text{A}, dI/dt=100\text{A}/\mu\text{s}, T_J=25^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	-	37	-	nC		

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. When mounted on minimum pad of 2 oz. copper
3. The power dissipation is limited by 150 $^\circ\text{C}$ junction temperature
4. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

CHARACTERISTIC CURVES

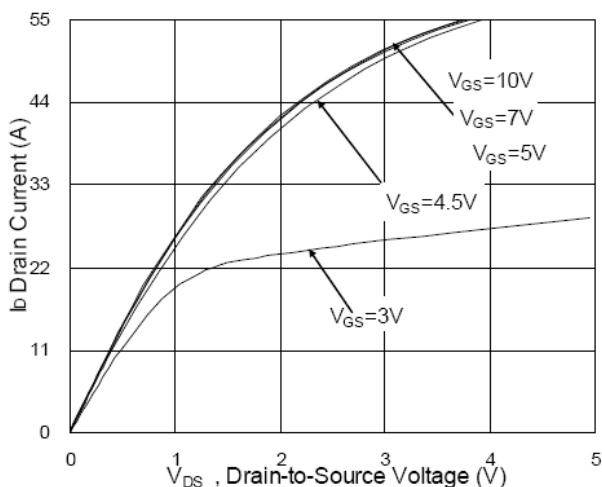


Fig.1 Typical Output Characteristics

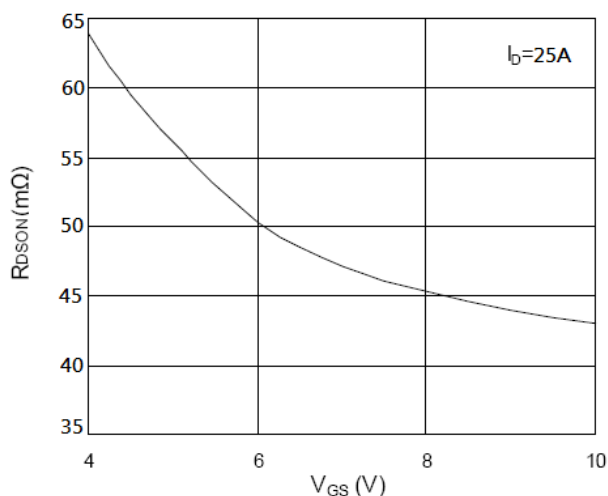


Fig.2 On-Resistance vs. Gate-Source

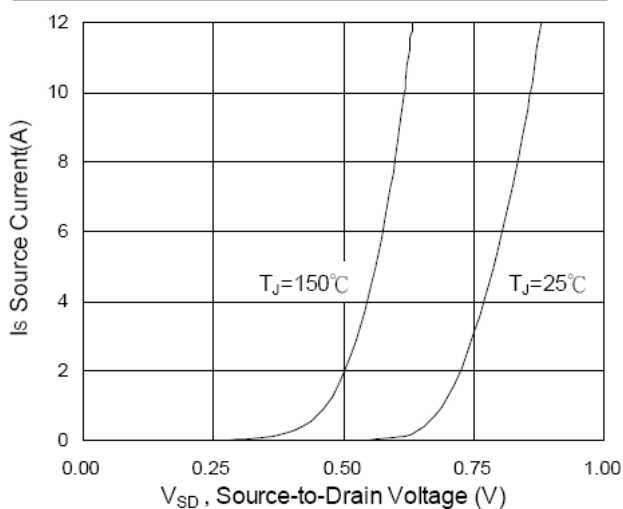


Fig.3 Forward Characteristics Of Reverse

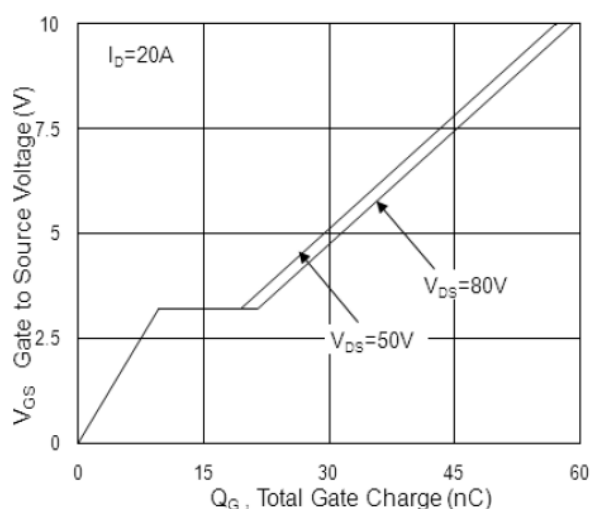


Fig.4 Gate-Charge Characteristics

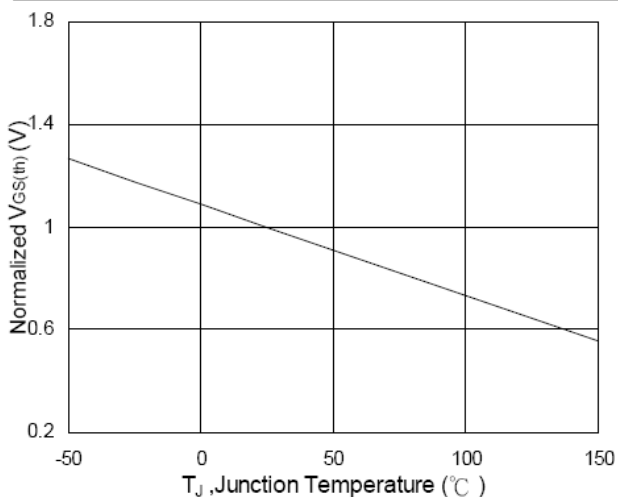


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

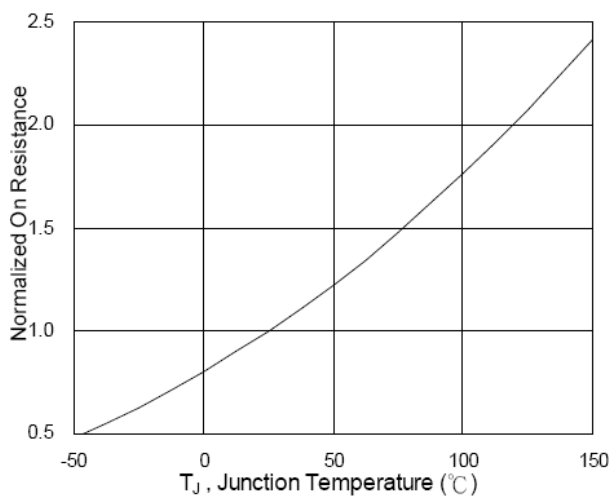


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

CHARACTERISTIC CURVES

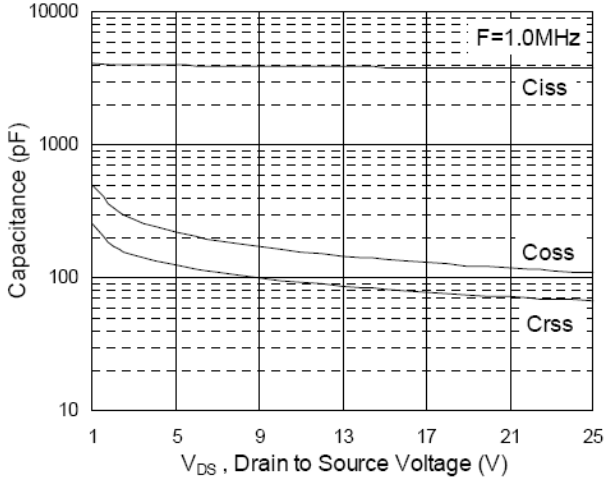


Fig.7 Capacitance

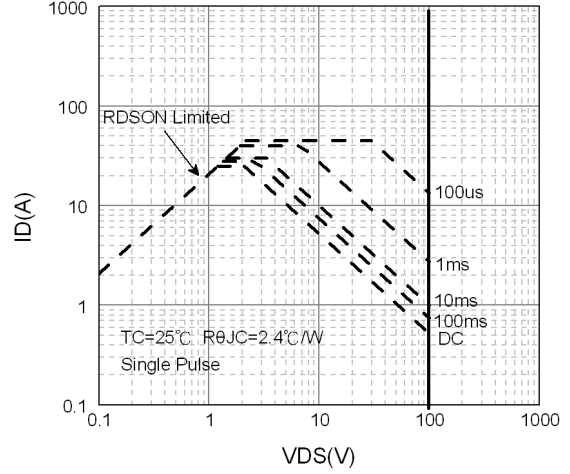


Fig.8 Safe Operating Area

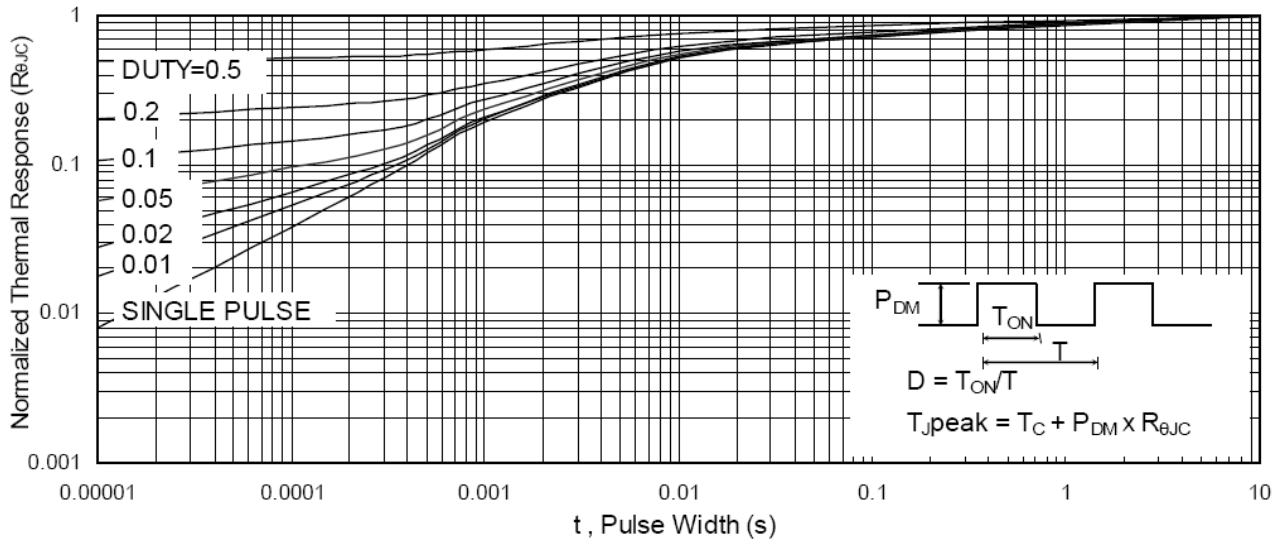


Fig.9 Normalized Maximum Transient Thermal Impedance

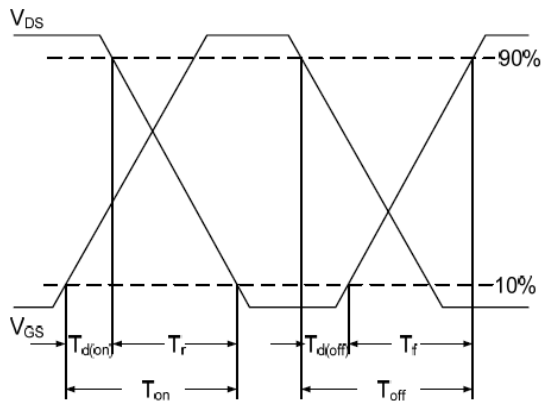


Fig.10 Switching Time Waveform

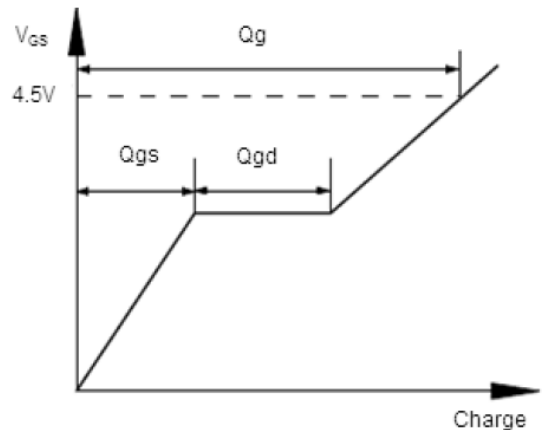


Fig.11 Gate Charge Waveform