Elektronische Bauelemente

SSD47N06-C

47A, 60V, $R_{DS(ON)}$ 12 mΩ
N-Ch Enhancement Mode Power MOSFET

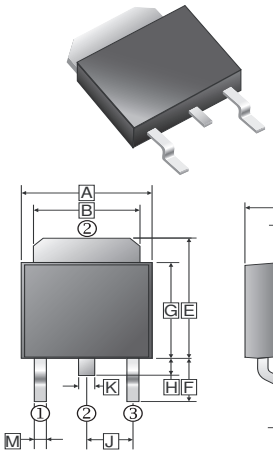
RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

SSD47N06-C is the highest performance trench N-ch MOSFETs with extreme high cell density, which provides excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

SSD47N06-C meets the RoHS and Green Product requirement with full function reliability approved.

TO-252(D-Pack)

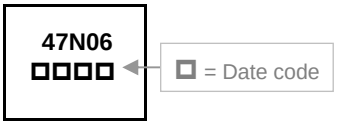


REF.	Millimeter Min.	Millimeter Max.	REF.	Millimeter Min.	Millimeter Max.
A	6.35	6.90	J	2.186	2.386
B	4.95	5.50	K	0.64	1.14
C	2.10	2.50	M	0.50	1.14
D	0.43	0.9	N	1.3	1.8
E	6.0	7.5	O	0	0.13
F	2.90 REF		P	0.58REF.	
G	5.40	6.40			
H	0.60	1.20			

FEATURES

- Advanced high cell density Trench technology
- Excellent Cdv/dt effect decline
- Green device available
- Super low gate charge

MARKING

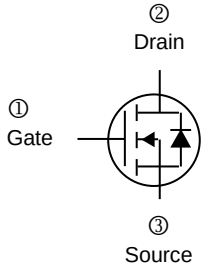


PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

ORDER INFORMATION

Part Number	Type
SSD47N06-C	Lead (Pb)-free and Halogen-free



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current@ V_{GS}=10V [1]	T_C=25℃	I_D	47	A
	T_C=100℃		30	
	T_A=25℃		9.2	
	T_A=70℃		7.5	
Pulsed Drain Current [2]		I_{DM}	100	A
Total Power Dissipation [3]	T_C=25℃	P_D	52	W
Maximum Thermal Resistance from Junction to Ambient [1]		$R_{\theta JA}$	62.5	℃/ W
Maximum Thermal Resistance from Junction to Case [1]		$R_{\theta JC}$	2.4	℃/ W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	℃

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage		BV_{DSS}	60	-	-	V	V_{GS}=0, I_D=250μA
Gate-Threshold Voltage		$V_{GS(th)}$	1	-	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transconductance		g_{fs}	-	42	-	S	V_{DS}=5V, I_D=30A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{DS}=0V, V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	1	μA	V_{DS}=48V, V_{GS}=0
	T_J=55℃		-	-	5		
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	-	12	mΩ	V_{GS}=10V, I_D=15A
			-	-	15		V_{GS}=4.5V, I_D=8A
Total Gate Charge		Q_g	-	28.7	-	nC	V_{DS}=48V V_{GS}=4.5V I_D=15A
Gate-Source Charge		Q_{gs}	-	10.5	-		
Gate-Drain (“Miller”) Charge		Q_{gd}	-	9.9	-		
Turn-on Delay Time		$T_{d(on)}$	-	10.4	-	nS	V_{DD}=30V V_{GS}=10V R_G=3.3Ω I_D=15A
Rise Time		T_r	-	9.2	-		
Turn-off Delay Time		$T_{d(off)}$	-	63	-		
Fall Time		T_f	-	4.8	-		
Input Capacitance		C_{iss}	-	3240	-	pF	V_{DS}=15V V_{GS}=0 f=1MHz
Output Capacitance		C_{oss}	-	210	-		
Reverse Transfer Capacitance		C_{rss}	-	146	-		
Source-Drain Diode Characteristics							
Diode Forward Voltage [2]		V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0
Continuous Source Current [1,4]		I_S	-	-	47	A	V_G=V_D=0V, Force Current
Pulsed Source Current [2,4]		I_{SM}	-	-	100	A	
Reverse Recovery Time		T_{RR}	-	18	-	nS	I_F=15A, dI/dt=100A/μs, T_J=25℃
Reverse Recovery Charge		Q_{RR}	-	14	-	nC	

Notes:

1. The data is tested with the surface of the device mounted on a 1 inch^2 FR4 board with 2OZ copper.
2. The data is tested by pulse: pulse with≤300μs, duty cycle ≤2%
3. The power dissipation is limited by 150℃ junct ion temperature.
4. The data is theoretically the same as I_D and I_{DM}; in real applications, it should be limited by the total power dissipation.

CHARACTERISTIC CURVE

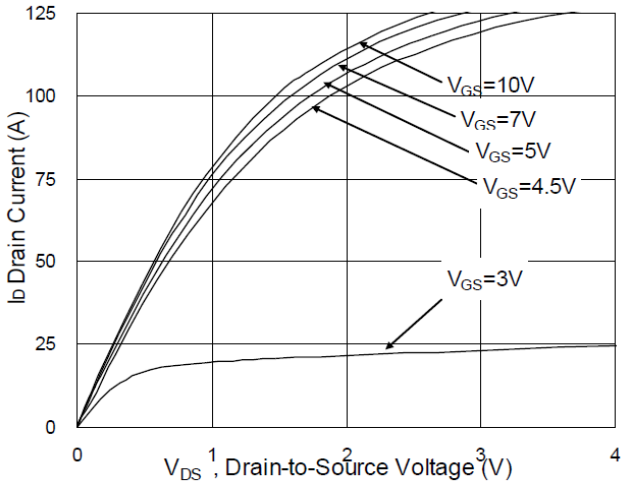


Fig.1 Typical Output Characteristics

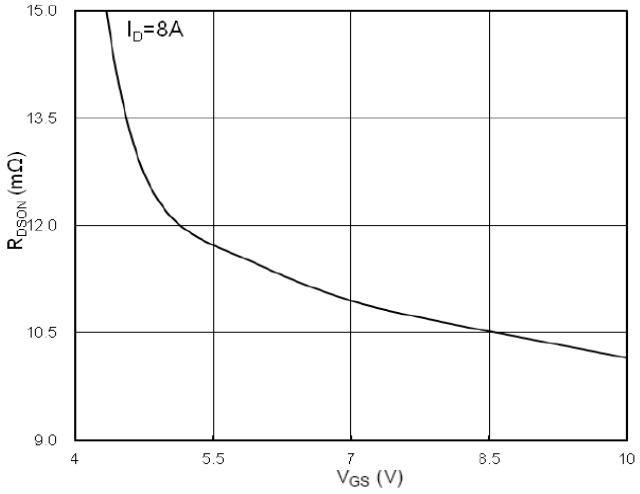


Fig.2 On-Resistance v.s Gate-Source

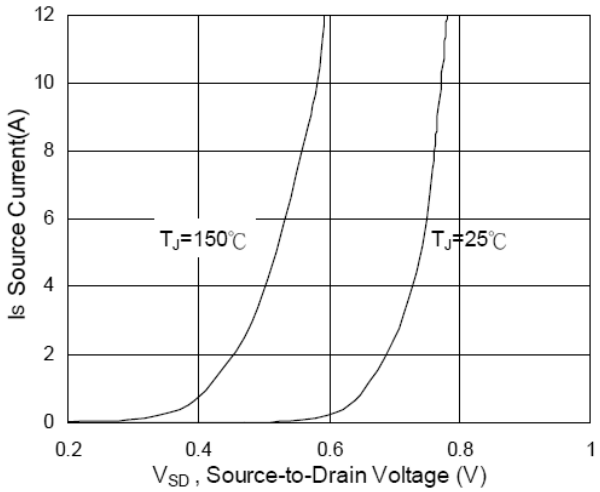


Fig.3 Forward Characteristics of Reverse

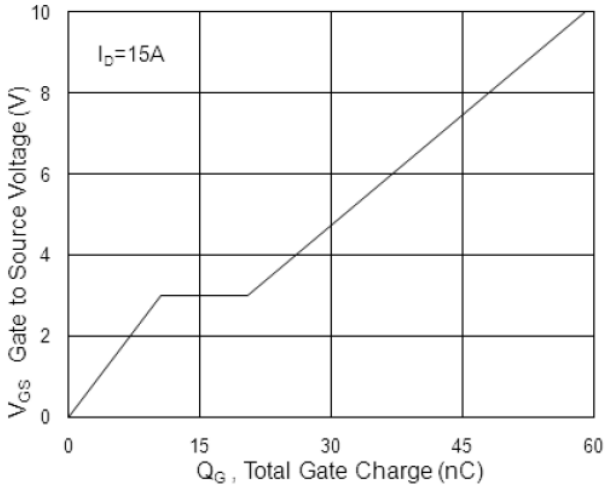


Fig.4 Gate-Charge Characteristics

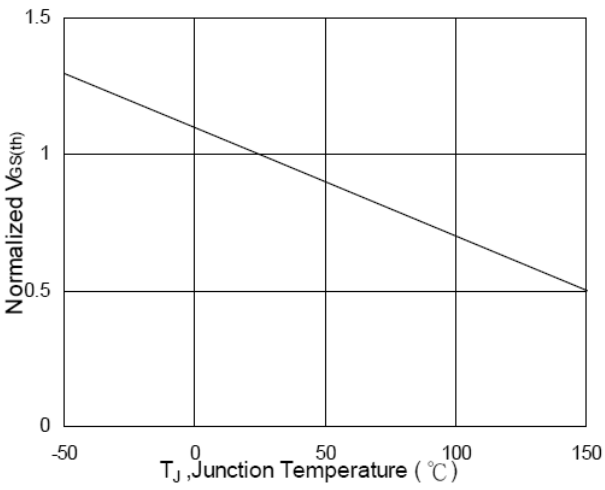


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

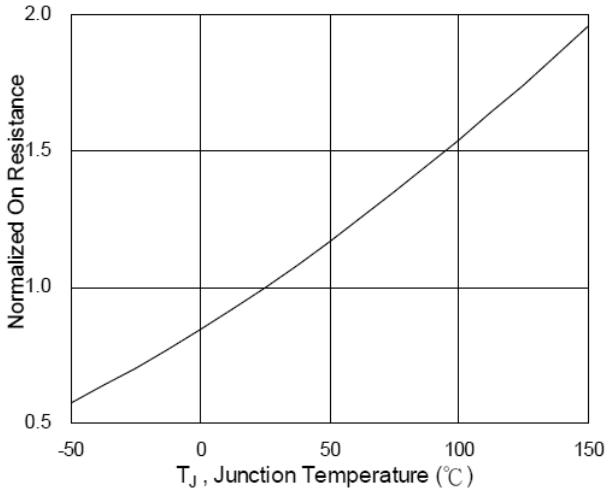


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVE

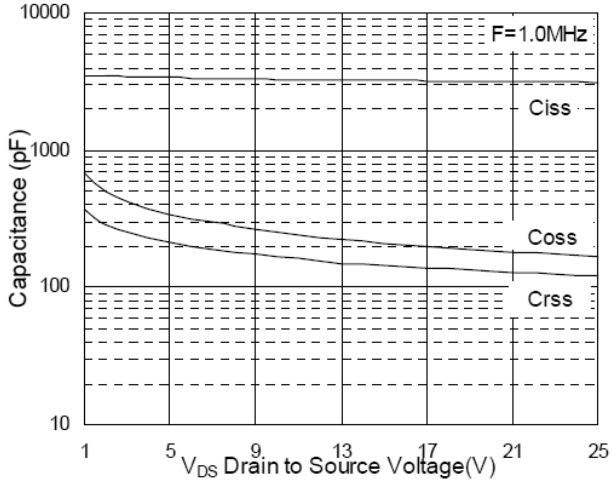


Fig.7 Capacitance

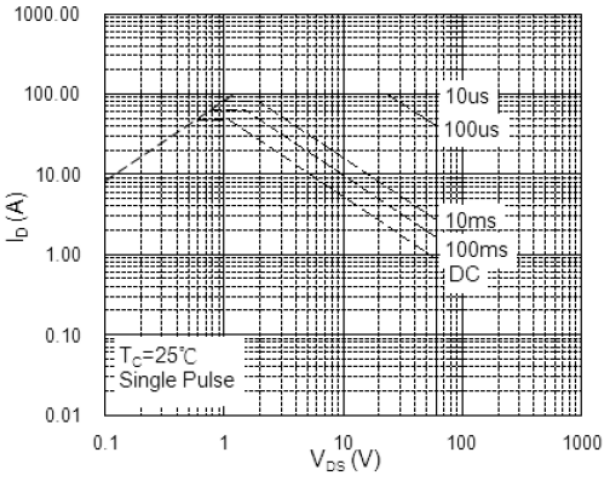


Fig.8 Safe Operating Area

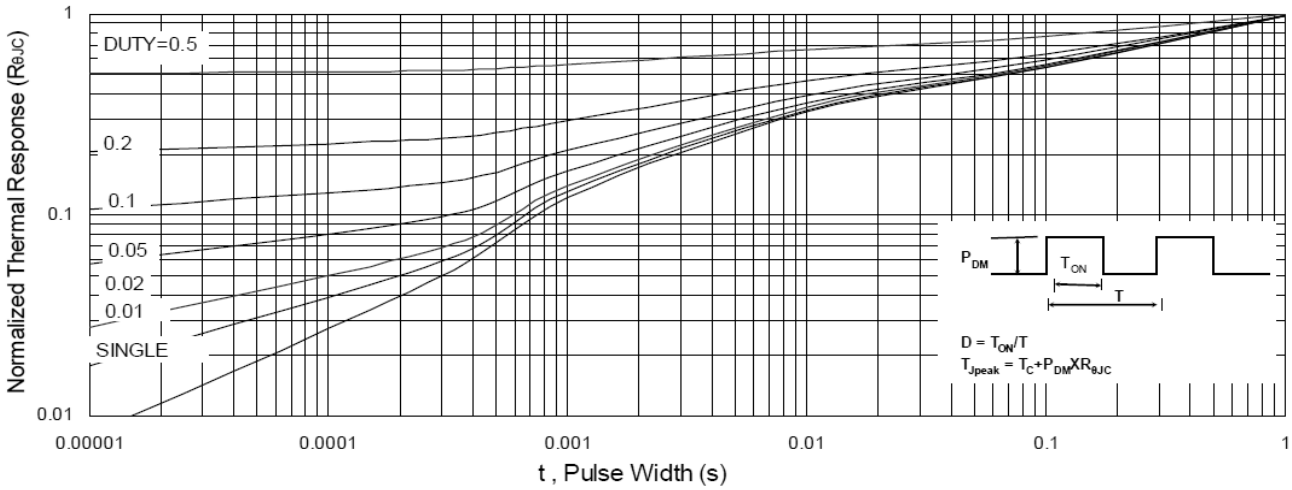


Fig.9 Normalized Maximum Transient Thermal Impedance

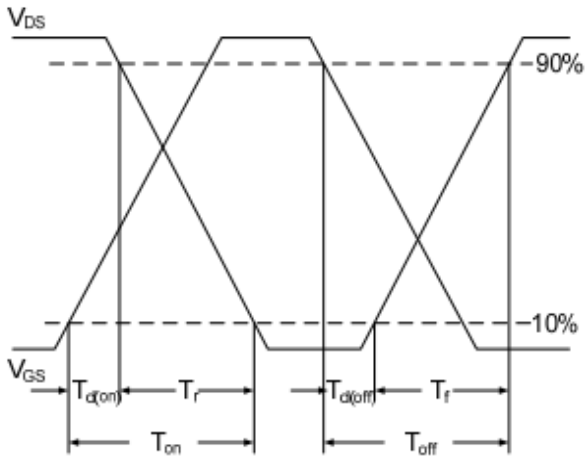


Fig.10 Switching Time Waveform

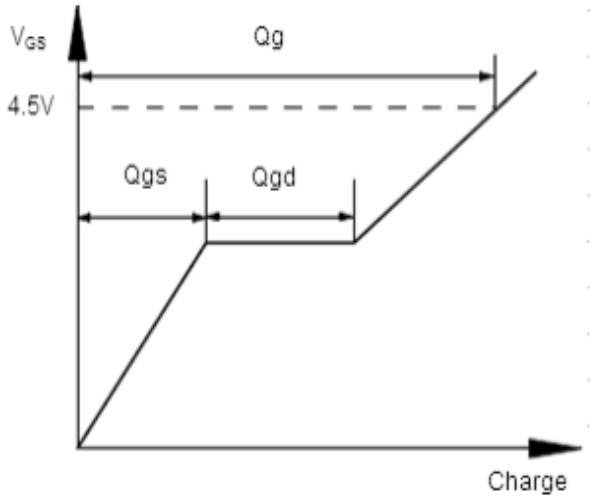


Fig.11 Gate Charge Waveform