

RoHS Compliant Product
 A suffix of "-C" specifies halogen free

DESCRIPTION

The SSD50N03-C is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications.

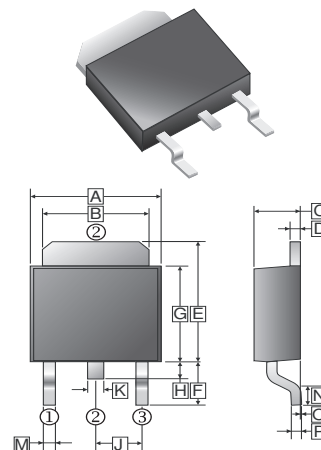
FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

MARKING



TO-252(D-Pack)



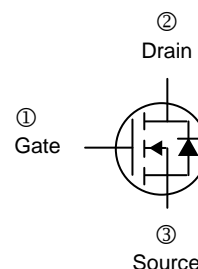
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.3	6.9	J	2.3	REF.
B	4.95	5.53	K	0.89	REF.
C	2.1	2.5	M	0.45	1.14
D	0.4	0.9	N	1.55	Typ.
E	6	7.7	O	0	0.15
F	2.90	REF.	P	0.58	REF.
G	5.4	6.4			
H	0.6	1.2			

PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

ORDER INFORMATION

Part Number	Type
SSD50N03-C	Lead (Pb)-free and Halogen-free



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, @ $V_{GS}=10V$ ¹	I_D	$T_C=25^\circ C$	51
		$T_C=100^\circ C$	36
		$T_A=25^\circ C$	12.4
		$T_A=70^\circ C$	10.3
Pulsed Drain Current ²	I_{DM}	110	A
Single Pulse Avalanche Energy ³	E_{AS}	128	mJ
Single Pulse Avalanche Current	I_{AS}	16	A
Total Power Dissipation ⁴	P_D	41	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ C$
Thermal Resistance Rating			
Maximum Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	3.05	$^\circ C/W$
Maximum Thermal Resistance Junction-ambient ¹	$R_{\theta JA}$	62.5	$^\circ C/W$

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ C$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS}=0, I_D=250\mu A$	
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$	
Forward Transconductance	g_{fs}	-	38	-	S	$V_{DS}=5V, I_D=30A$	
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 20V$	
Drain-Source Leakage Current	I_{DSS}	$T_J=25^\circ C$	-	-	1	μA	$V_{DS}=24V, V_{GS}=0$
		$T_J=55^\circ C$	-	-	5		
Static Drain-Source On-Resistance ⁴	$R_{DS(ON)}$	-	-	9	m Ω	$V_{GS}=10V, I_D=30A$	
		-	-	13.5		$V_{GS}=4.5V, I_D=15A$	
Total Gate Charge	Q_g	-	12.6	-	nC	$I_D=15A$ $V_{DS}=15V$ $V_{GS}=4.5V$	
Gate-Source Charge	Q_{gs}	-	4.2	-			
Gate-Drain ("Miller") Charge	Q_{gd}	-	5.1	-			
Turn-on Delay Time	$T_{d(on)}$	-	4.6	-	nS	$V_{DD}=15V$ $I_D=15A$ $V_{GS}=10V$ $R_D=3.3 \Omega$	
Rise Time	T_r	-	12.2	-			
Turn-off Delay Time	$T_{d(off)}$	-	26.6	-			
Fall Time	T_f	-	8	-			
Input Capacitance	C_{iss}	-	1317	-	pF	$V_{GS}=0$ $V_{DS}=15V$ $f=1.0MHz$	
Output Capacitance	C_{oss}	-	163	-			
Reverse Transfer Capacitance	C_{rss}	-	131	-			
Guaranteed Avalanche Characteristics							
Single Pulse Avalanche Energy ⁵	E_{AS}	32	-	-	mJ	$V_{DD}=25V, L=1mH, I_{AS}=8A$	
Source-Drain Diode							
Continuous Source Current ¹	I_S	-	-	51	A		
Pulsed Source Current ²	I_{SM}	-	-	110			
Diode Forward Voltage ⁴	V_{SD}	-	-	1.2	V	$I_S=1A, V_{GS}=0$	
Reverse Recovery Time	T_{rr}	-	9.2	-	nS	$I_F=30A, di/dt=100A/\mu s$	
Reverse Recovery Charge	Q_{rr}	-	2	-	nC	$T_J=25^\circ C$	

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. Pulse width limited by maximum junction temperature , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=1mH, I_{AS}=16A$.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
5. The Min. value is 100% EAS tested guarantee.

CHARACTERISTIC CURVES

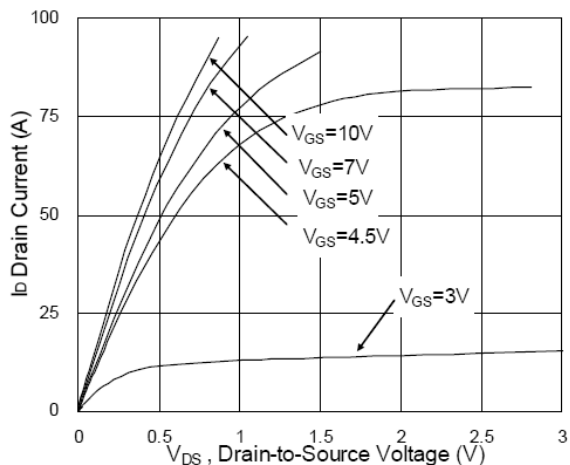


Fig.1 Typical Output Characteristics

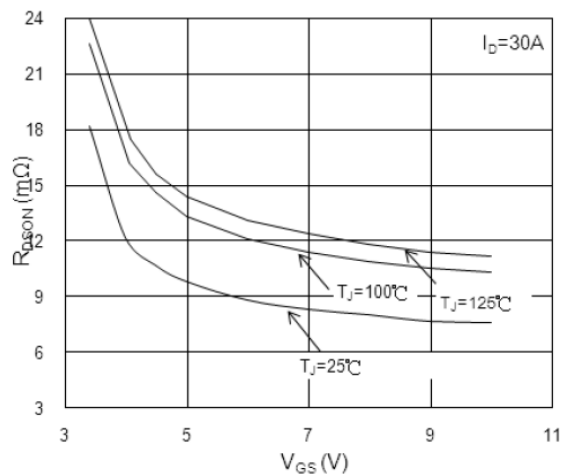


Fig.2 On-Resistance vs. G-S Voltage

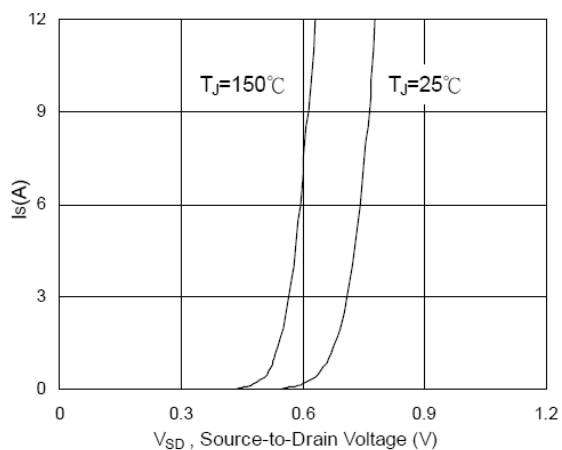


Fig.3 Forward Characteristics of Reverse

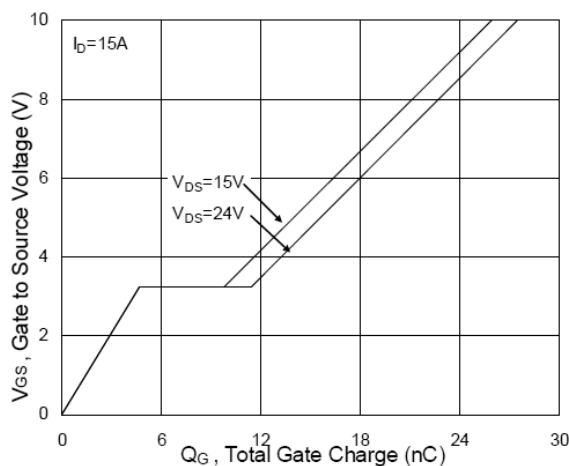


Fig.4 Gate-Charge Characteristics

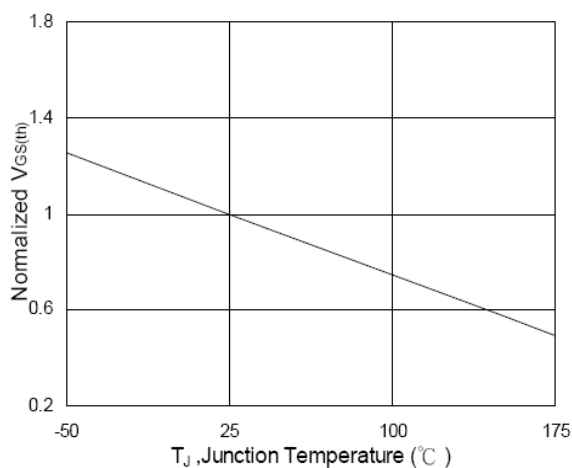


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

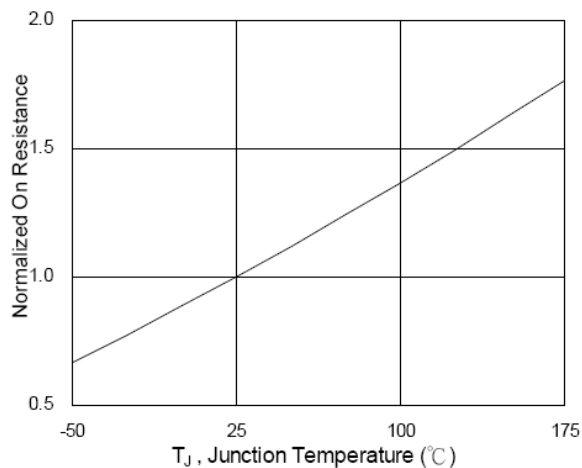


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

CHARACTERISTIC CURVES

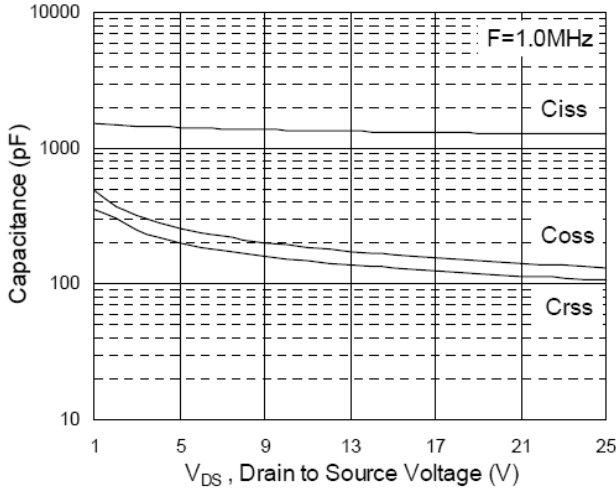


Fig.7 Capacitance

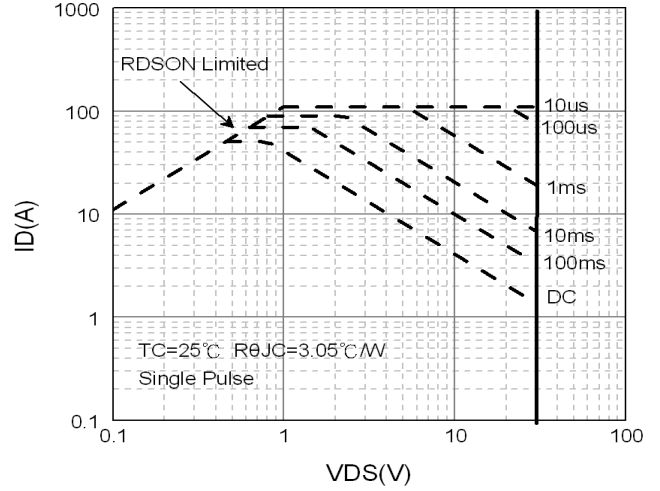


Fig.8 Safe Operating Area

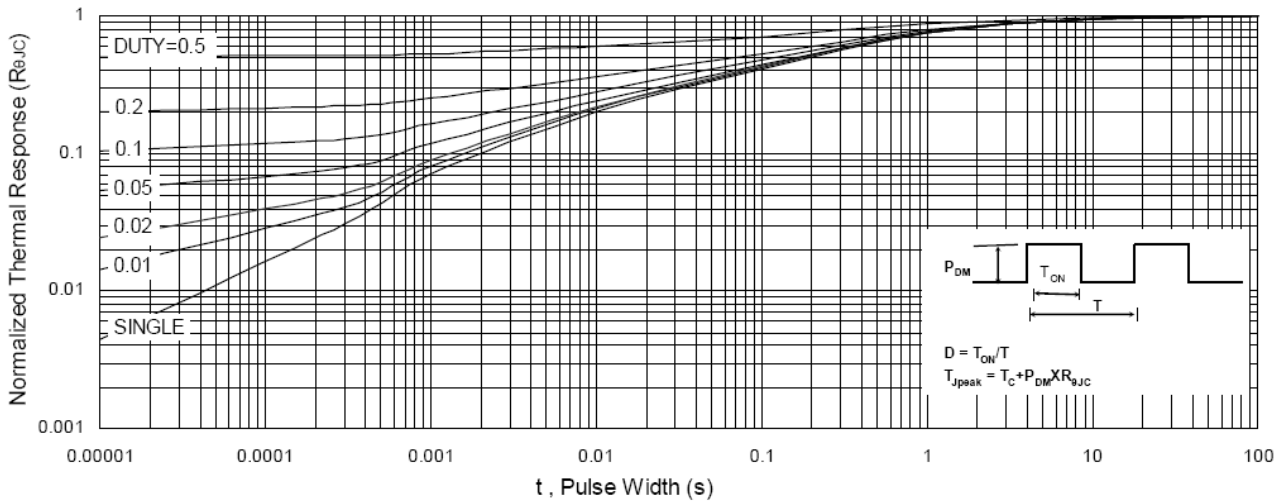


Fig.9 Normalized Maximum Transient Thermal Impedance

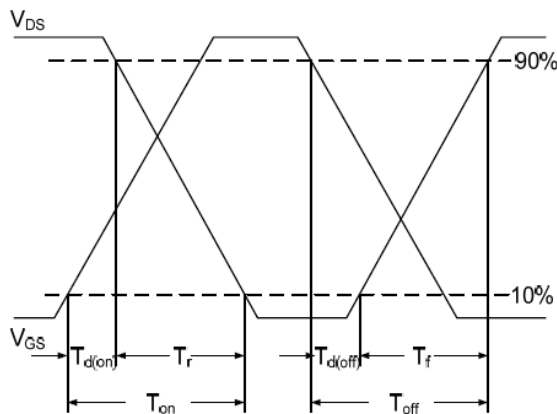


Fig.10 Switching Time Waveform

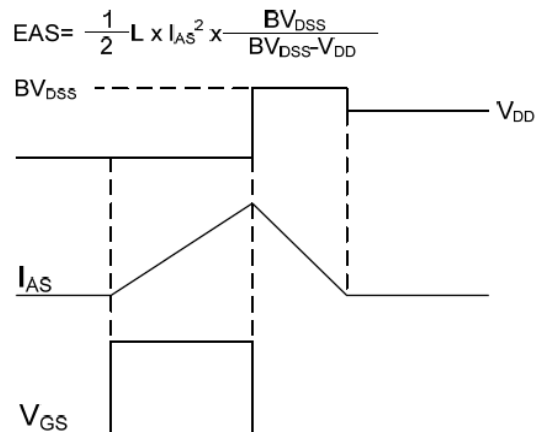


Fig.11 Unclamped Inductive Switching Waveform