Elektronische Bauelemente

SSD50P04-C

-50A, -40V, $R_{DS(ON)}$ 13mΩ

P-Ch Enhancement Mode Power MOSFET

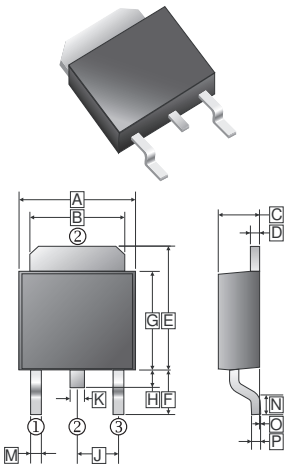
RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSD50P04-C is the highest performance trench P-Ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSD50P04-C meet the RoHS and Green Product Requirement.

TO-252(D-Pack)



FEATURES

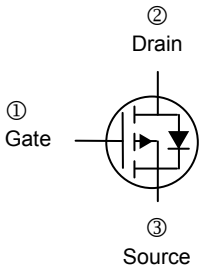
- Advanced high Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

ORDER INFORMATION

Part Number	Type
SSD50P04-C	Lead (Pb)-free and Halogen-free



REF.	Millimeter Min.	Millimeter Max.	REF.	Millimeter Min.	Millimeter Max.
A	6.3	6.9	J	2.3 REF.	
B	4.95	5.53	K	0.89 REF.	
C	2.1	2.5	M	0.45	1.14
D	0.4	0.9	N	1.55 Typ.	
E	6	7.7	O	0	0.15
F	2.90 REF		P	0.58 REF.	
G	5.4	6.4			
H	0.6	1.2			

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current @V_{GS}=10V [1]	T_C=25°C	I_D	-50	A
	T_C=100°C		-32	
	T_A=25°C		-10	
	T_A=70°C		-8	
Pulsed Drain Current [2]		I_{DM}	-105	A
Power Dissipation [3]	T_C=25°C	P_D	52	W
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 ~150	°C
Thermal Resistance Ratings				
Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	62	°C / W
Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	2.4	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Drain-Source Breakdown Voltage		BV_{DSS}	-40	-	-	V	V_{GS}=0V, I_D= -250μA
Gate Threshold Voltage		$V_{GS(th)}$	-1	-	-2.5	V	V_{DS}=V_{GS}, I_D= -250μA
Forward Transfer conductance		g_{fs}	-	24	-	S	V_{DS}= -5V, I_D= -18A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V, V_{DS}=0V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	-1	μA	V_{DS}= -32V, V_{GS}=0V
	T_J=55°C		-	-	-5		
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	10.5	13	mΩ	V_{GS}= -10V, I_D= -18A
			-	15	20		V_{GS}= -4.5V, I_D= -12A
Total Gate Charge		Q_g	-	27.9	-	nC	I_D= -12A V_{DS}= -20V V_{GS}= -4.5V
Gate-Source Charge		Q_{gs}	-	7.7	-		
Gate-Drain Change		Q_{gd}	-	7.5	-		
Turn-on Delay Time		$T_{d(on)}$	-	40	-	nS	V_{DD}= -15V I_D= -1A V_{GS}= -10V R_G=3.3Ω
Rise Time		T_r	-	35.2	-		
Turn-off Delay Time		$T_{d(off)}$	-	100	-		
Fall Time		T_f	-	9.6	-		
Input Capacitance		C_{iss}	-	3500	-	pF	V_{GS}=0V V_{DS}= -15V f=1MHz
Output Capacitance		C_{oss}	-	323	-		
Reverse Transfer Capacitance		C_{rss}	-	222	-		
Source-Drain Diode							
Continuous Source Current [1]		I_S	-	-	-50	A	V_{GS}=V_{DS}=0V
Pulsed Source Current [2]		I_{SM}	-	-	-105	A	
Diode Forward Voltage [2]		V_{SD}	-	-	-1	V	T_J=25°C, I_S= -1A, V_{GS}=0V

Notes:
1. The date tested by surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width≦300us, duty cycle≦2%.
3. The power dissipation is limited by 150℃ junction temperature.

TYPICAL CHARACTERISTICS CURVE

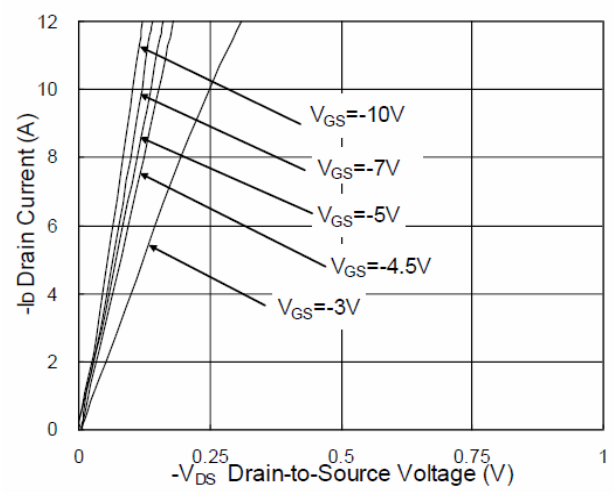


Fig.1 Typical Output Characteristics

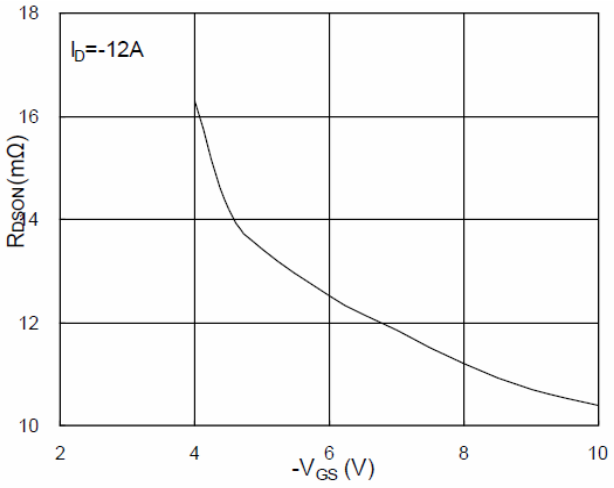


Fig.2 On-Resistance v.s Gate-Source

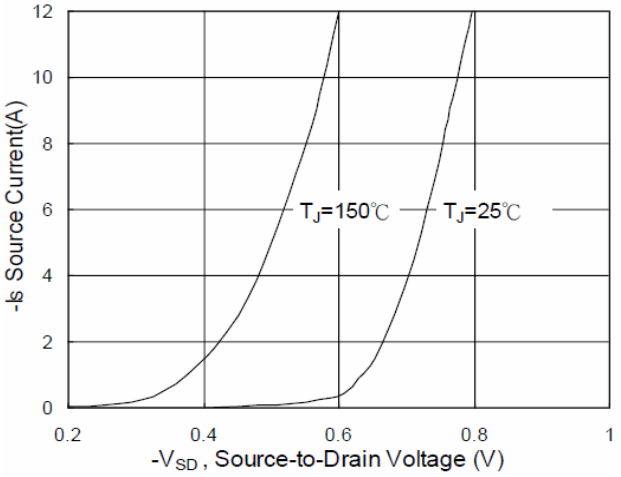


Fig.3 Forward Characteristics Of Reverse

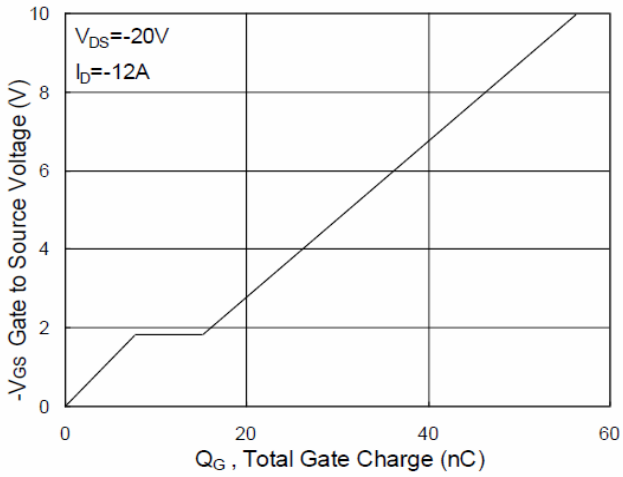


Fig.4 Gate-Charge Characteristics

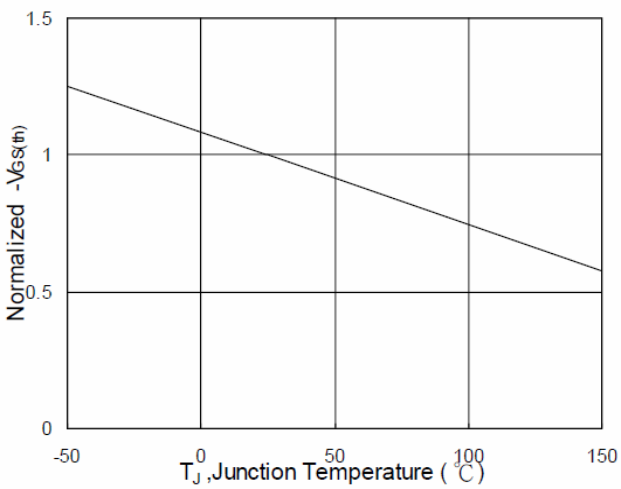


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

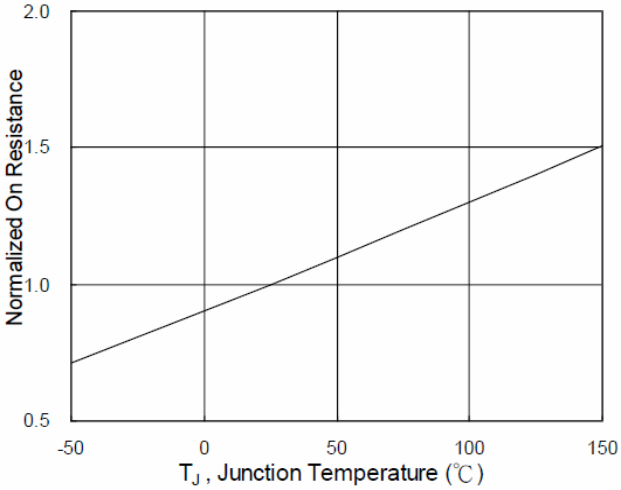


Fig.6 Normalized R_{DSON} v.s T_J

TYPICAL CHARACTERISTICS CURVE

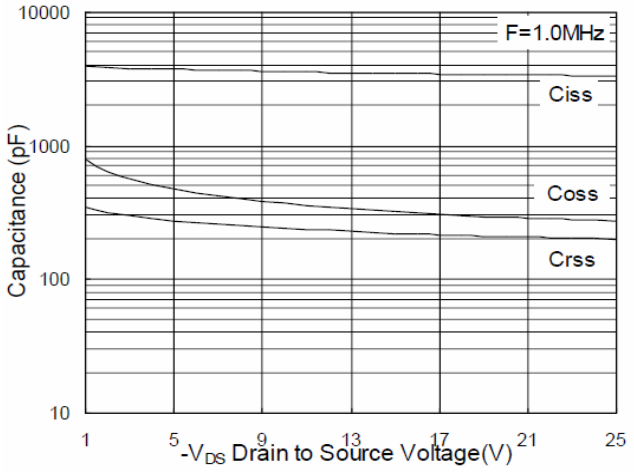


Fig.7 Capacitance

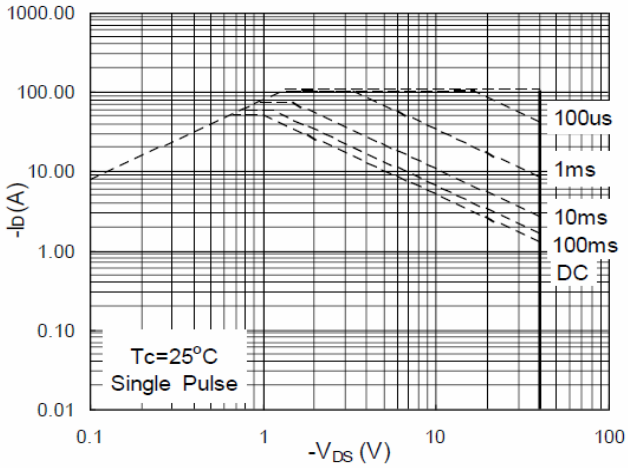


Fig.8 Safe Operating Area

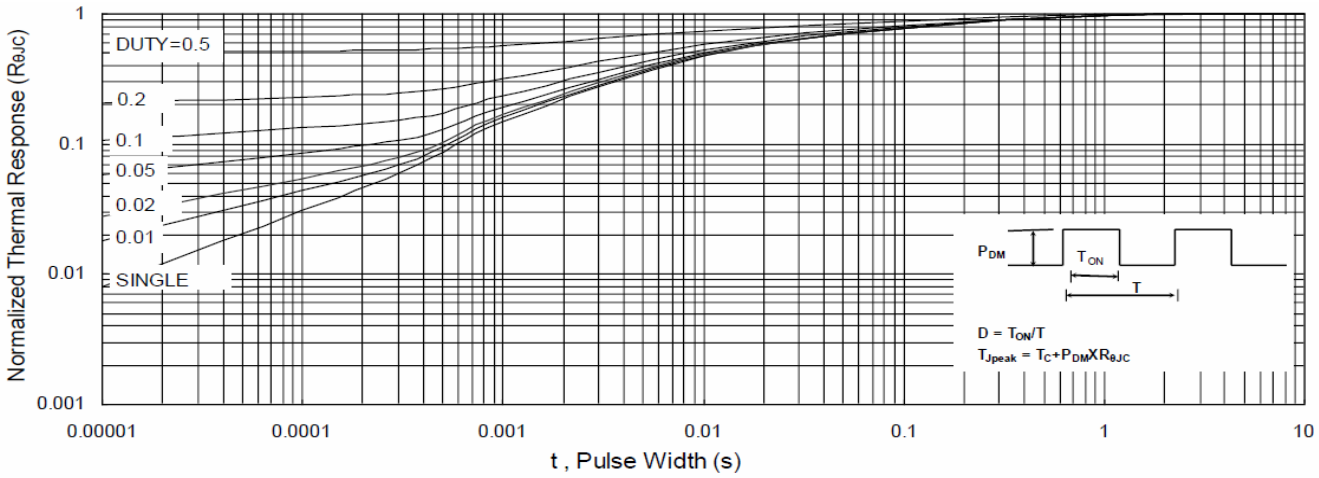


Fig.9 Normalized Maximum Transient Thermal Impedance

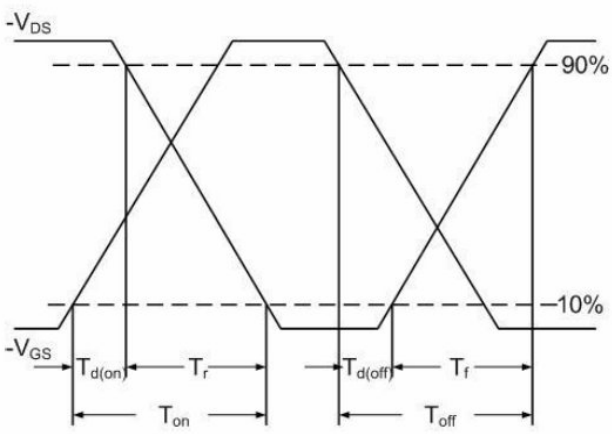


Fig.10 Switching Time Waveform

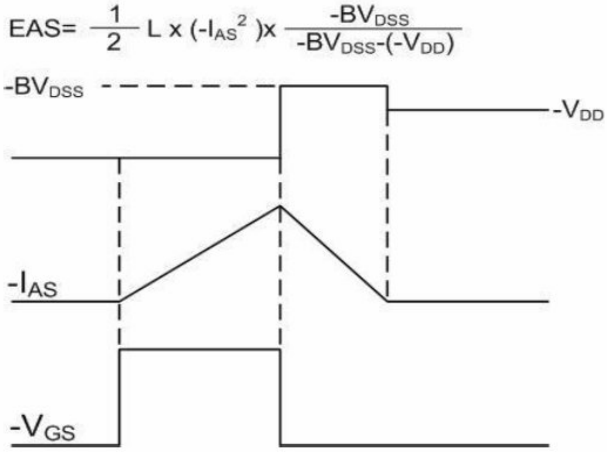


Fig.11 Unclamped Inductive Waveform