

RoHS Compliant Product  
A suffix of "-C" specifies halogen free

## DESCRIPTION

SSD56N45S-C is the highest performance trench N-ch MOSFETs with extreme high cell density, which provides excellent  $R_{DS(ON)}$  and gate charge for most of the synchronous buck converter applications.

SSD56N45S-C meets the RoHS and Green Product requirement with full function reliability approved.

## FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Green Device Available

## MARKING



## PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

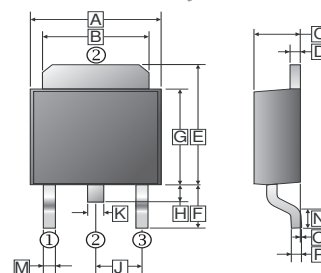
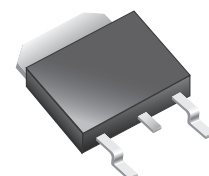
## ORDER INFORMATION

Part Number	Type
SSD56N45S-C	Lead (Pb)-free and Halogen-free

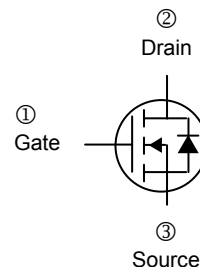
## ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	45	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup> @ $V_{GS}=10\text{V}$	$I_D$	$T_C=25^\circ\text{C}$	56
		$T_C=100^\circ\text{C}$	39
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	150	A
Power Dissipation	$P_D$	52	W
Operating Junction & Storage Temperature	$T_J, T_{STG}$	-55~150	$^\circ\text{C}$
<b>Thermal Resistance Ratings</b>			
Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	2.4	

## TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	J	2.30	REF.
B	5.20	5.50	K	0.64	0.90
C	2.15	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.65
E	6.8	7.5	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.25			
H	0.64	1.20			



**ELECTRICAL CHARACTERISTICS** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	$BV_{DSS}$	45	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$
Gate-Threshold Voltage	$V_{GS(th)}$	1	1.55	2.2	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 20\text{V}$
Drain-Source Leakage Current	$I_{DSS}$	-	-	1	uA	$V_{DS}=36\text{V}, V_{GS}=0, T_J=25^\circ\text{C}$
		-	-	100		$V_{DS}=36\text{V}, V_{GS}=0, T_J=100^\circ\text{C}$
Static Drain-Source On-Resistance <sup>3</sup>	$R_{DS(ON)}$	-	7.5	9.5	m $\Omega$	$V_{GS}=10\text{V}, I_D=20\text{A}$
		-	10	14		$V_{GS}=4.5\text{V}, I_D=10\text{A}$
Transconductance	$g_{fs}$	-	25	-	S	$V_{DS}=5\text{V}, I_D=20\text{A}$
Gate Resistance	$R_g$	-	1.5	-	$\Omega$	$V_{DS}=V_{GS}=0, f=1.0\text{MHz}$
Total Gate Charge (4.5V)	$Q_g$	-	7	-	nC	$I_D=10\text{A}$ $V_{DD}=20\text{V}$ $V_{GS}=10\text{V}$
Total Gate Charge		-	14.5	-		
Gate-Source Charge		-	2	-		
Gate-Drain Change		-	2.5	-		
Turn-on Delay Time	$T_{d(on)}$	-	6	-	nS	$V_{DD}=20\text{V}$ $I_D=10\text{A}$ $V_{GS}=10\text{V}$ $R_G=10\Omega$
Rise Time	$T_r$	-	5	-		
Turn-off Delay Time	$T_{d(off)}$	-	21	-		
Fall Time	$T_f$	-	5	-		
Input Capacitance	$C_{iss}$	-	942	-	pF	$V_{GS}=0$ $V_{DS}=20\text{V}$ $f=1.0\text{MHz}$
Output Capacitance	$C_{oss}$	-	309	-		
Reverse Transfer Capacitance	$C_{rss}$	-	29	-		
<b>Source-Drain Diode</b>						
Diode Forward Voltage <sup>3</sup>	$V_{SD}$	-	-	1.2	V	$I_S=20\text{A}, V_{GS}=0$
Reverse Recovery Time	$T_{rr}$	-	24	-	nS	$I_F=10\text{A}, V_R=20\text{V}, di/dt=200\text{A}/\mu\text{s}$
Reverse Recovery Charge	$Q_{rr}$	-	19	-	nC	

Notes:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The Pulse width limited by maximum junction temperature, Pulse Width  $\leq 10\mu\text{s}$ , Duty Cycle  $\leq 2\%$
3. The Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$

**CHARACTERISTIC CURVES**

Fig 1. Typical Output Characteristics

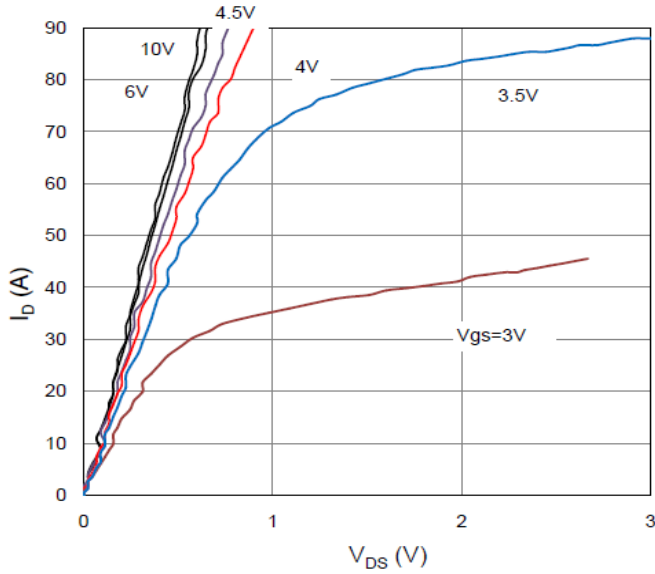


Figure 2. On-Resistance vs. Gate-Source Voltage

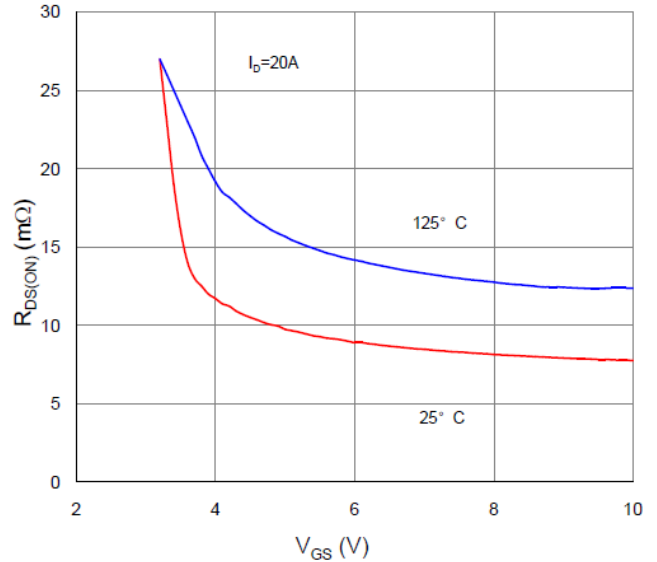


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

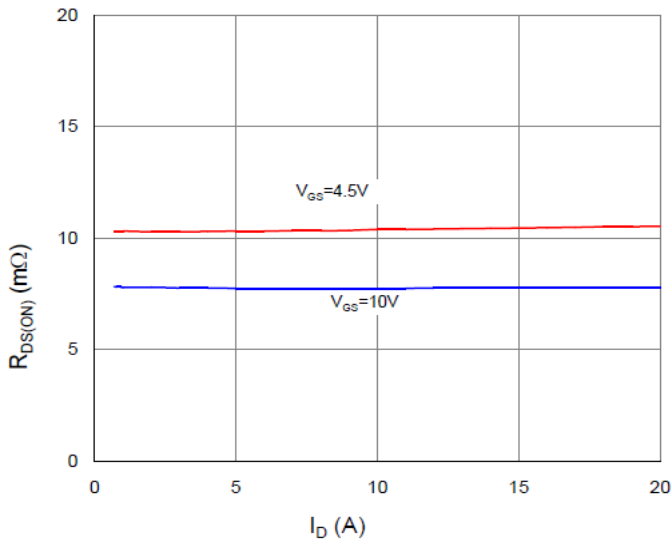


Figure 4. Normalized On-Resistance vs. Junction Temperature

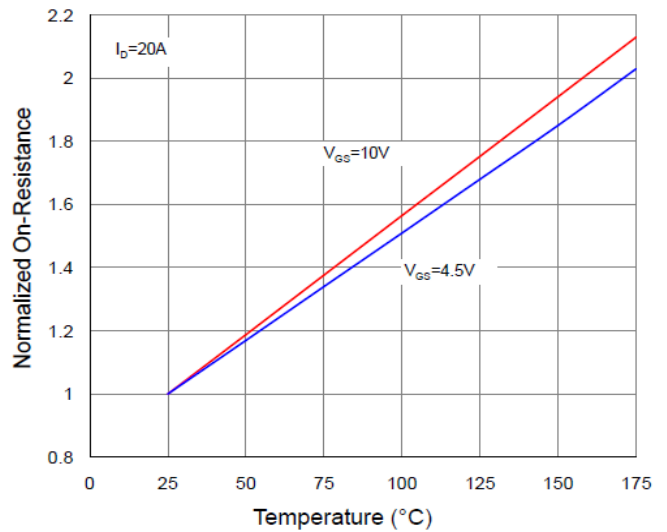


Figure 5. Typical Transfer Characteristics

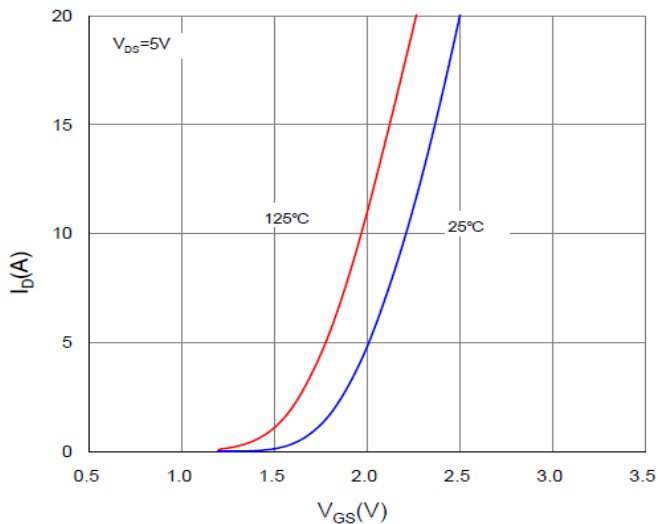
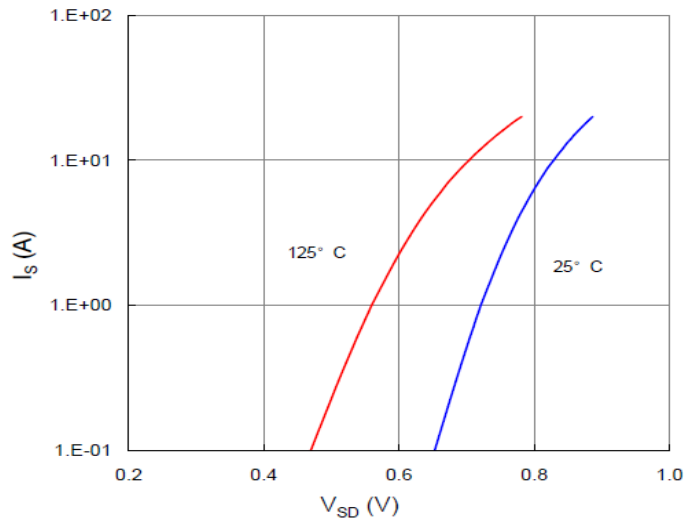


Figure 6. Typical Source-Drain Diode Forward Voltage



**CHARACTERISTIC CURVES**

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

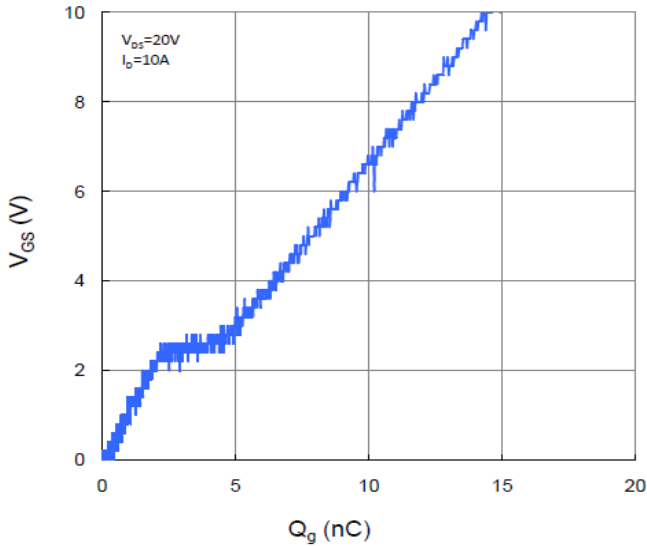


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

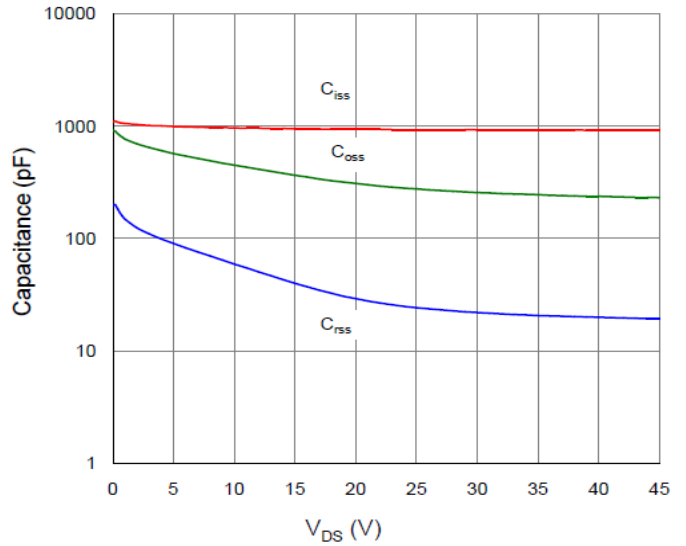


Figure 9. Maximum Safe Operating Area

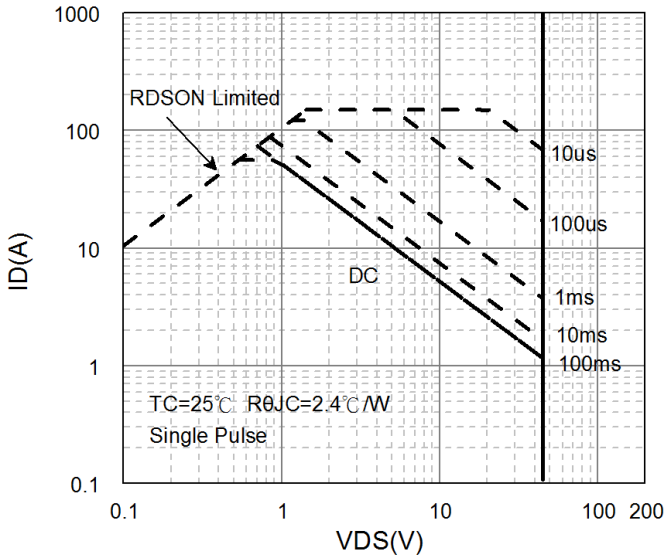


Figure 10. Drain Current vs Case Temperature

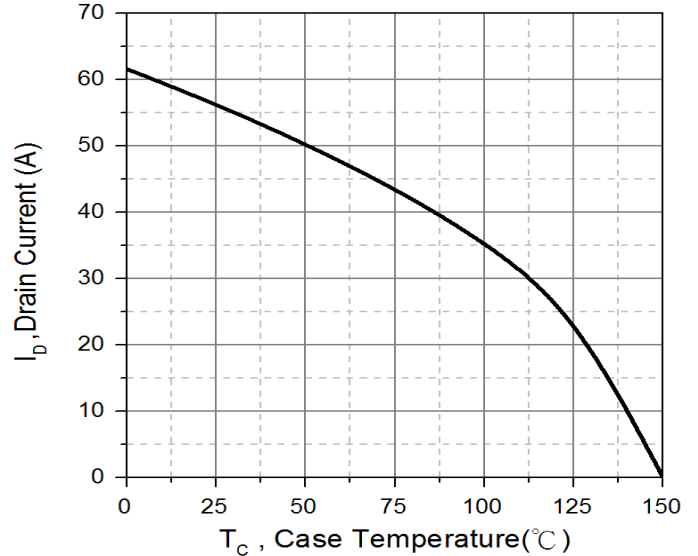


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

