

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSU04N65 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications .

FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

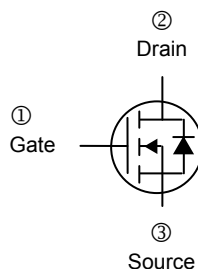
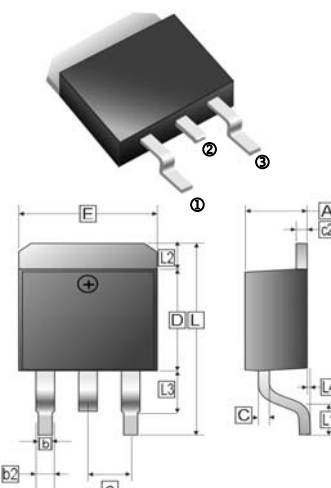
MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-263	0.8K	13 inch

TO-263



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.00	4.85	c2	1.10	1.45
b	0.68	1.00	b2	1.34	REF
L4	0.00	0.30	D	8.0	9.15
C	0.36	0.53	e	2.54	REF
L3	1.50	REF	L	14.6	15.85
L1	2.29	2.79	L2	1.27	REF
E	9.60	10.45			

ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current @ $V_{GS}=10V$ ¹	I_D	$T_C=25^\circ\text{C}$	4
		$T_C=100^\circ\text{C}$	2.6
Pulsed Drain Current ²	I_{DM}	8	A
Total Power Dissipation ⁴	P_D	$T_C=25^\circ\text{C}$	112
		$T_A=25^\circ\text{C}$	2
Single Pulse Avalanche Energy ³	E_{AS}	2.36	mJ
Single Pulse Avalanche Current	I_{AS}	2	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Rating			
Maximum Thermal Resistance Junction-Ambient (PCB mount) ¹	$R_{\theta JA}$	62	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	1.12	$^\circ\text{C} / \text{W}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	650	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$
Gate-Threshold Voltage	$V_{GS(th)}$	2	-	5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Forward Transconductance	g_{fs}	-	3	-	S	$V_{DS}=15\text{V}, I_D=2\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 30\text{V}$
Drain-Source Leakage Current	I_{DSS}	-	-	2	μA	$V_{DS}=520\text{V}, V_{GS}=0$
Static Drain-Source On-Resistance ²	$R_{DS(ON)}$	-	2.1	2.6	Ω	$V_{GS}=10\text{V}, I_D=2\text{A}$
Gate Resistance	R_G	-	3.4	6.8	Ω	$V_{DS}=V_{GS}=0, f=1\text{MHz}$
Total Gate Charge(10V)	Q_g	-	18	-	nC	$I_D=1\text{A}$ $V_{DS}=520\text{V}$ $V_{GS}=10\text{V}$
Gate-Source Charge	Q_{gs}	-	4.9	-		
Gate-Drain ("Miller") Change	Q_{gd}	-	6.1	-		
Turn-on Delay Time	$T_{d(on)}$	-	11.2	-	nS	$V_{DD}=300\text{V}$ $I_D=1\text{A}$ $V_{GS}=10\text{V}$ $R_G=10\Omega$
Rise Time	T_r	-	18.8	-		
Turn-off Delay Time	$T_{d(off)}$	-	29.2	-		
Fall Time	T_f	-	29.2	-		
Input Capacitance	C_{iss}	-	775	-	pF	$V_{GS}=0$ $V_{DS}=25\text{V}$ $f=1.0\text{MHz}$
Output Capacitance	C_{oss}	-	56	-		
Reverse Transfer Capacitance	C_{rss}	-	3.8	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy ⁵	EAS	0.6	-	-	mJ	$V_{DD}=100\text{V}, L=1\text{mH}, I_{AS}=1\text{A}$
Source-Drain Diode						
Diode Forward Voltage ²	V_{SD}	-	-	1	V	$I_S=1\text{A}, V_{GS}=0$
Reverse Recovery Time	T_{rr}	-	195	-	ns	$I_F=1\text{A}, T_J=25^\circ\text{C},$ $di/dt=100\text{A}/\mu\text{S}$
Reverse Recovery Charge	Q_{rr}	-	580	-	nC	
Continuous Source Current ^{1,6}	I_S	-	-	4	A	$V_D=V_G=0, \text{Force Current}$
Pulsed Source Current ^{2,6}	I_{SM}	-	-	8	A	

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2oz copper.
- The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating . The test condition is $V_{DD}=100\text{V}, V_{GS}=10\text{V}, L=1\text{mH}, I_{AS}=2\text{A}$
- The power dissipation is limited by 150°C , junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

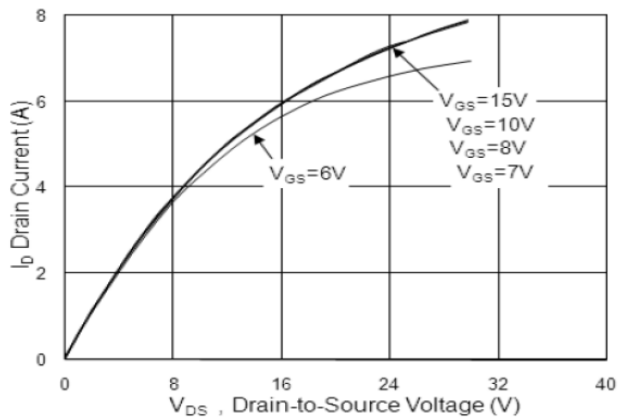


Fig.1 Typical Output Characteristics

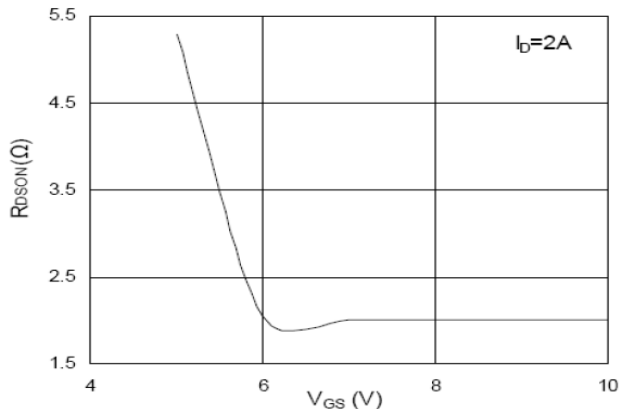


Fig.2 On-Resistance vs. G-S Voltage

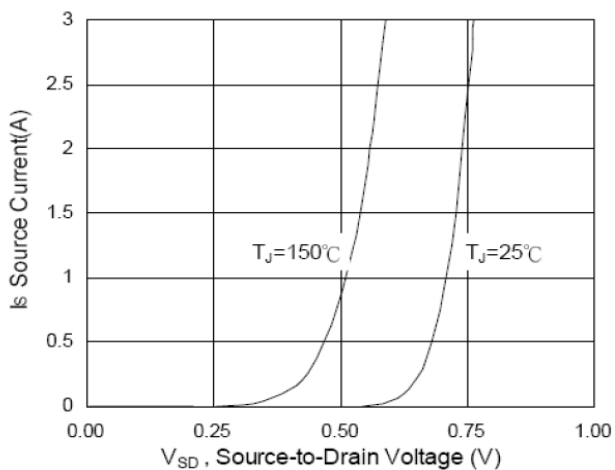


Fig.3 Forward Characteristics of Reverse

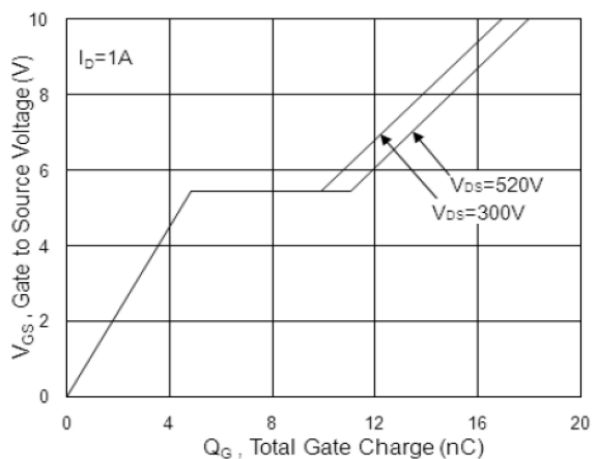


Fig.4 Gate-Charge Characteristics

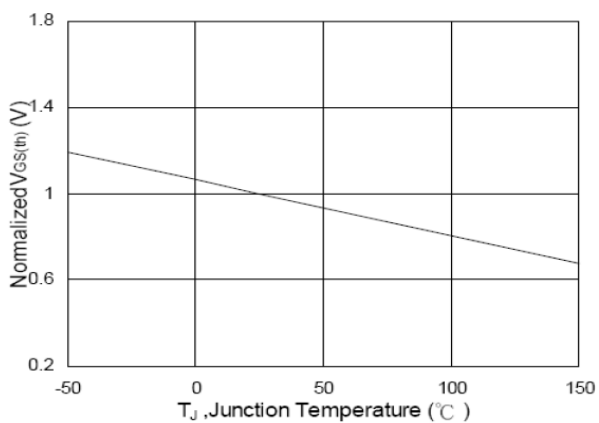


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

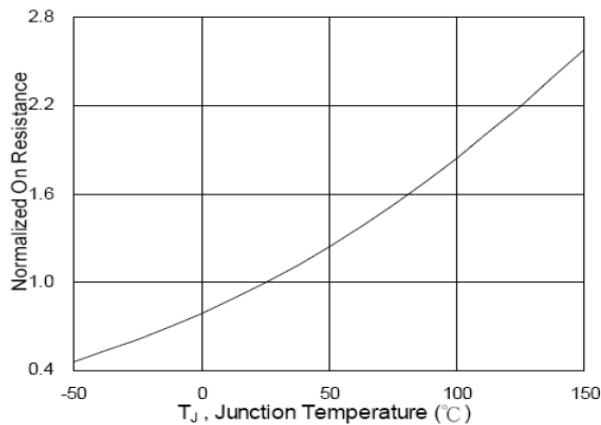


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

CHARACTERISTIC CURVES

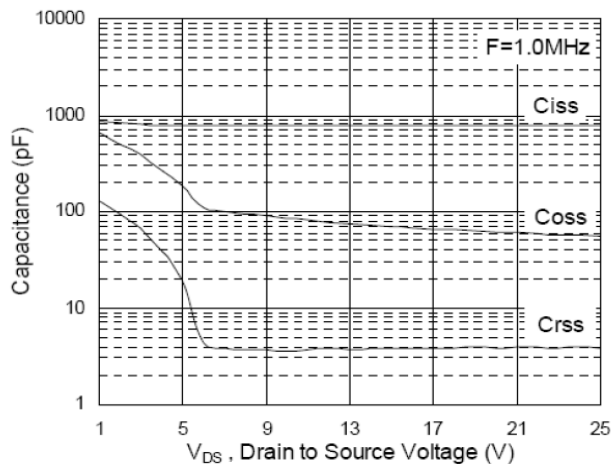


Fig.7 Capacitance

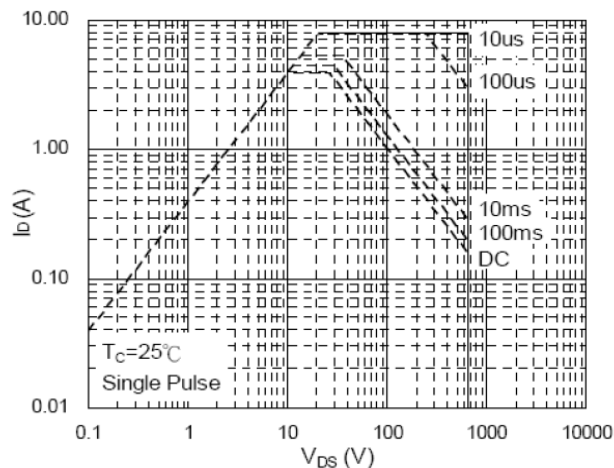


Fig.8 Safe Operating Area

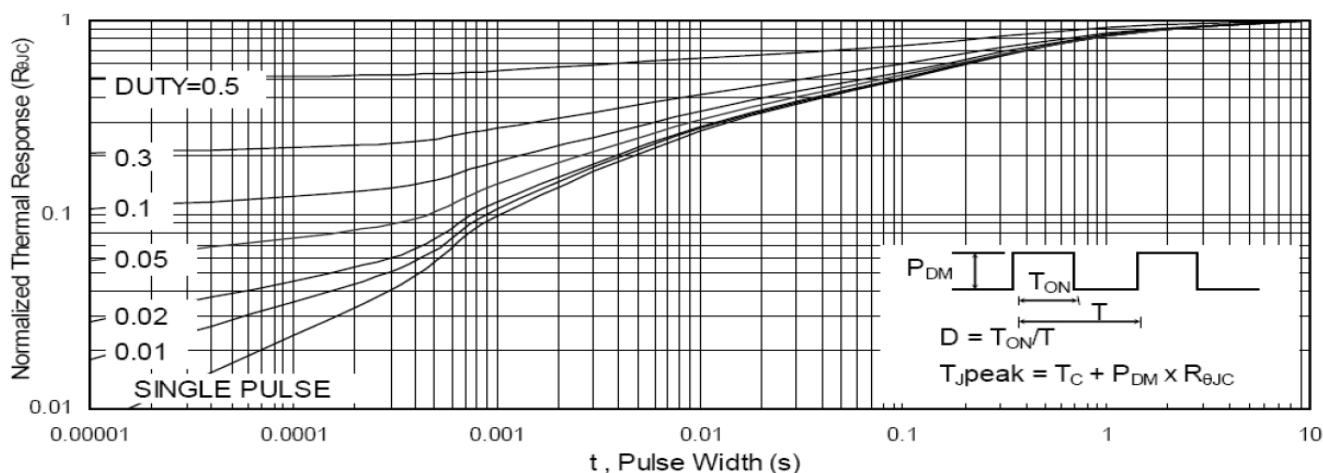


Fig.9 Normalized Maximum Transient Thermal Impedance

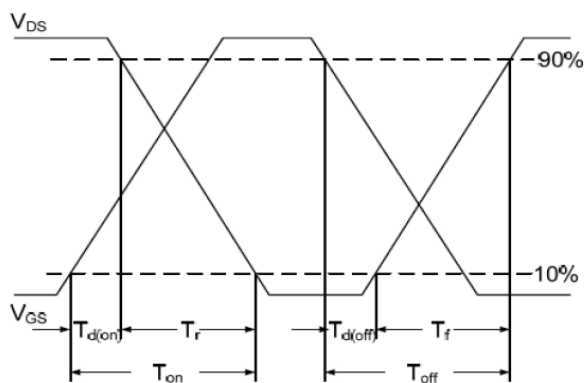


Fig.10 Switching Time Waveform

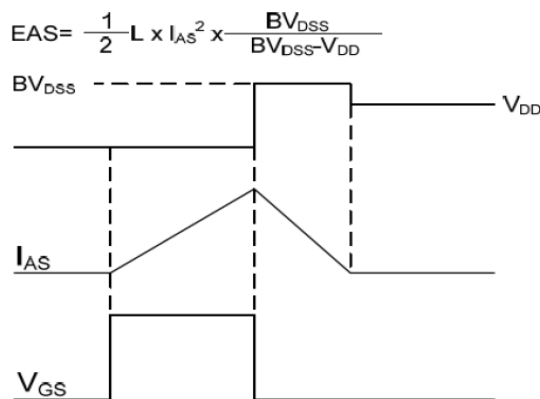


Fig.11 Unclamped Inductive Switching Waveform