Elektronische Bauelemente

SSU50N10-C

54A, 100V, $R_{DS(ON)}$ 22mΩ

N-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSU50N10-C is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Excellent CdV/dt Effect Decline
- 100% E_{AS} and 100% R_g Guaranteed
- Green Device Available

MARKING

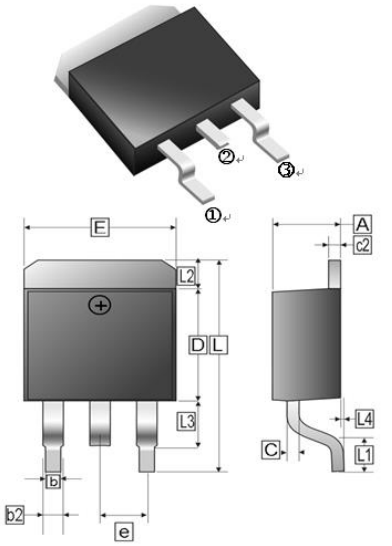
PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-263	0.8K	13 inch

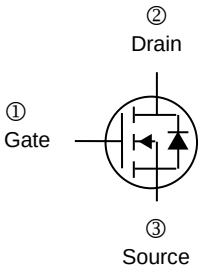
ORDER INFORMATION

Part Number	Type
SSU50N10-C	Lead (Pb)-free and Halogen-free

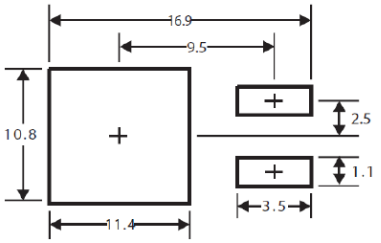
TO-263



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.00	4.87	c2	1.07	1.65
b	0.51	1.01	b2	1.34 REF	
L4	0.00	0.30	D	8.0	9.65
C	0.30	0.74	e	2.54 REF	
L3	1.50 REF		L	14.6	16.1
L1	2.5 REF		L2	1.27 REF	
E	9.60	10.67			



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1] @V_{GS}=10V	T_C=25°C	I_D	54	A
	T_C=100°C		38	
Pulsed Drain Current [2]		I_{DM}	160	A
Total Power Dissipation [4]	T_C=25°C	P_D	104	W
	T_A=25°C		3.13	
Single Pulse Avalanche Energy [3]		E_{AS}	338	mJ
Single Pulse Avalanche Current		I_{AS}	26	A
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	°C
Thermal Resistance Rating				
Maximum Thermal Resistance Junction-Ambient (PCB mount) [1]		$R_{\theta JA}$	40	°C/W
Maximum Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	1.2	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	100	-	-	V	V_{GS}=0, I_D=250μA
Gate-Threshold Voltage		$V_{GS(th)}$	2	-	4	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transconductance		g_{fs}	-	27	-	S	V_{DS}=5V, I_D=30A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	1	μA	V_{DS}=80V, V_{GS}=0
	T_J=55°C		-	-	5		
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	18	22	mΩ	V_{GS}=10V, I_D=30A
			-	36	40		V_{GS}=7V, I_D=15A
Gate Resistance		R_g	-	0.6	3.8	Ω	V_{DS}=0, V_{GS}=15mV, f=1MHz
Total Gate Charge		Q_g	-	27.6	38.6	nC	I_D=30A V_{DS}=80V V_{GS}=10V
Gate-Source Charge		Q_{gs}	-	11.4	16		
Gate-Drain (“Miller”) Change		Q_{gd}	-	7.9	11.1		
Turn-on Delay Time		$T_{d(on)}$	-	15.6	31.2	nS	V_{DS}=50V I_D=30A V_{GS}=10V R_G=3.3Ω
Rise Time		T_r	-	17.2	31		
Turn-off Delay Time		$T_{d(off)}$	-	16.8	33.6		
Fall Time		T_f	-	9.2	18.4		
Input Capacitance		C_{iss}	-	1890	2645	pF	V_{GS}=0 V_{DS}=15V f=1MHz
Output Capacitance		C_{oss}	-	268	375		
Reverse Transfer Capacitance		C_{rss}	-	67	94		
Single Pulse Avalanche Energy [5]		E_{AS}	121	-	-	mJ	V_{DD}=50V, L=1mH, I_{AS}=15.6A
Source-Drain Diode							
Diode Forward Voltage [2]		V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0
Continuous Source Current [1,6]		I_S	-	-	40	A	V_D=V_G=0, Force Current
Reverse Recovery Time		T_{rr}	-	34	-	ns	I_F=30A, T_J=25°C dI/dt=100A/μs
Reverse Recovery Charge		Q_{rr}	-	47	-	nC	

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width≦ 300μs, duty cycle≦ 2%.
3. The E_{AS} data shows Max. rating. The test condition is V_{DD}=50V, V_{GS}=10V, L=1mH, I_{AS}=26A.
4. The power dissipation is limited by 150°C junction temperature.
5. The Min. value is 100% E_{AS} tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

CHARACTERISTIC CURVES

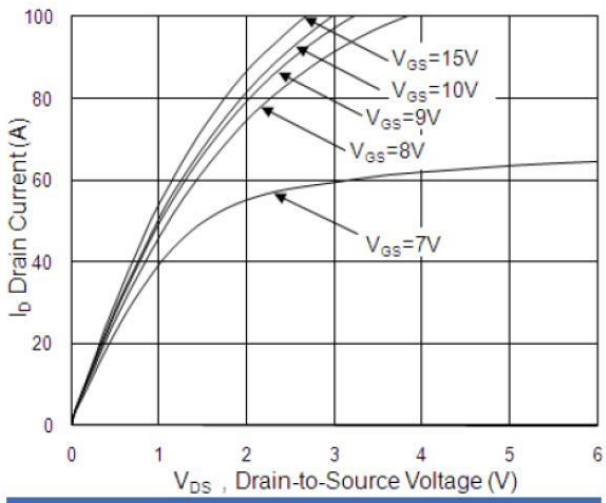


Fig.1 Typical Output Characteristics

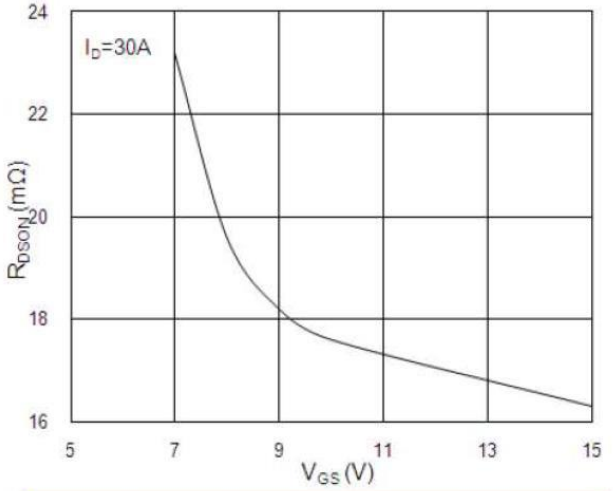


Fig.2 On-Resistance v.s Gate-Source

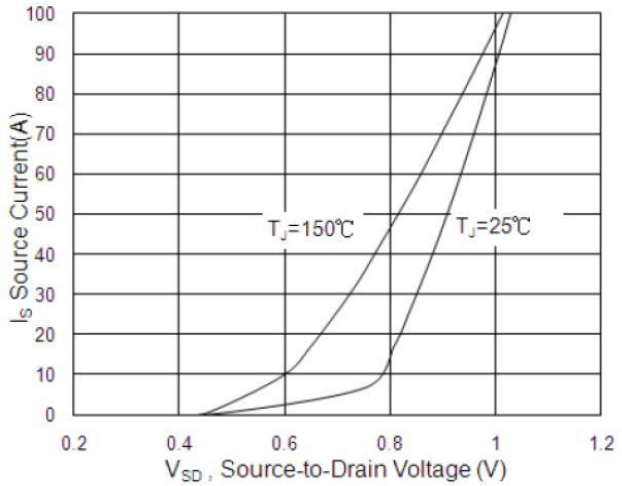


Fig.3 Forward Characteristics of Reverse

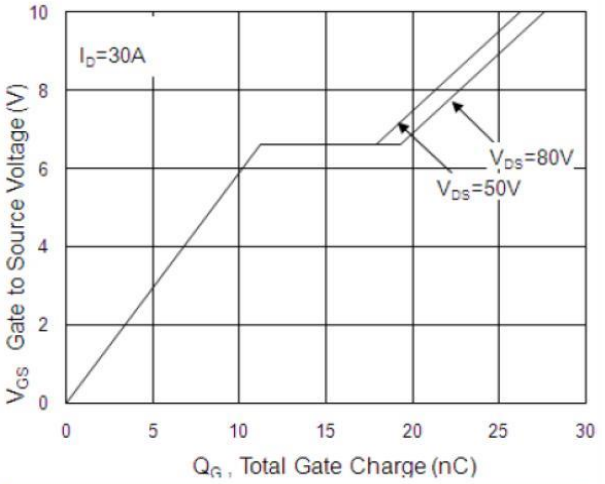


Fig.4 Gate-Charge Characteristics

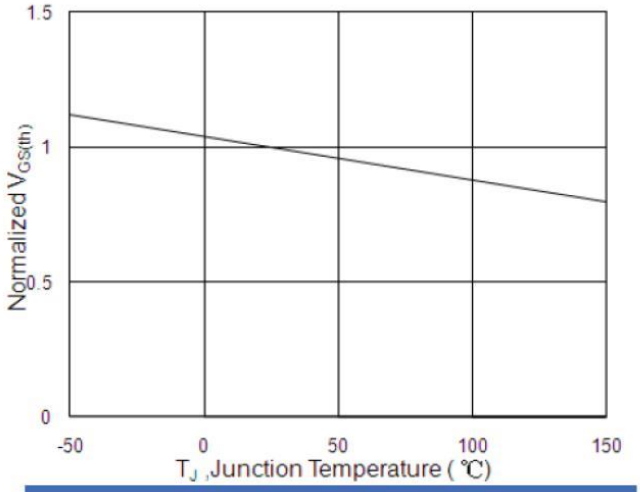


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

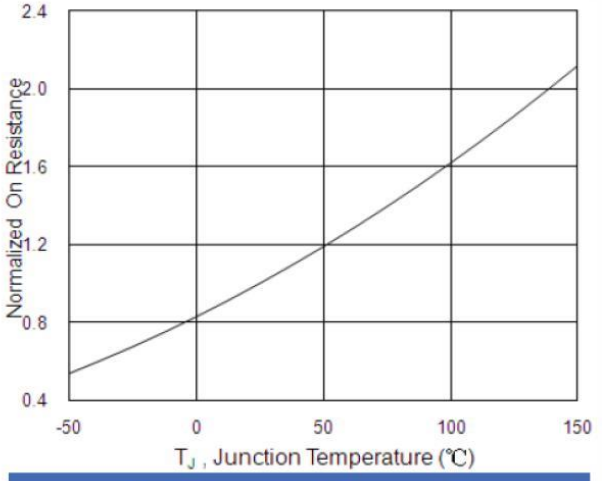


Fig.6 Normalized R_{DSON} v.s T_J

CHARACTERISTIC CURVES

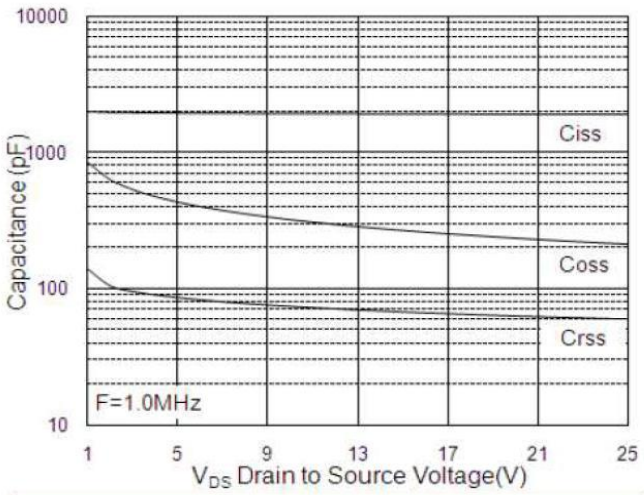


Fig.7 Capacitance

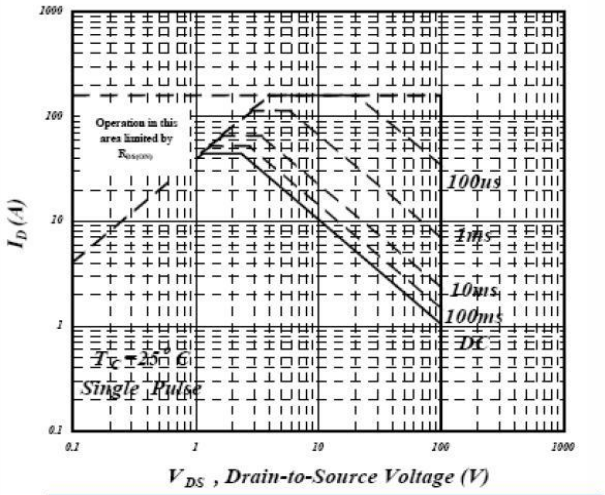


Fig.8 Safe Operating Area

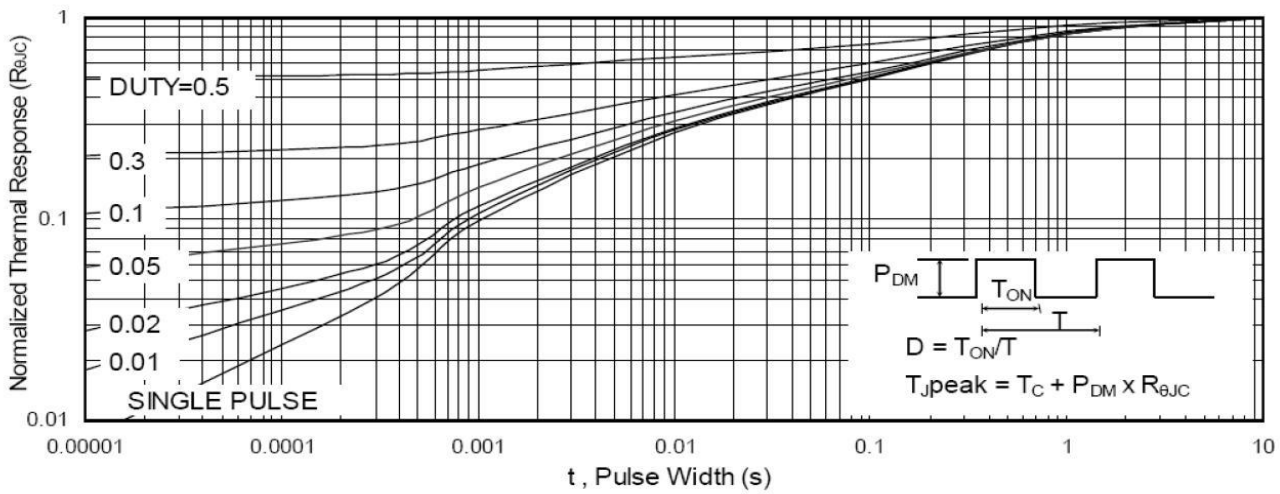


Fig.9 Normalized Maximum Transient Thermal Impedance

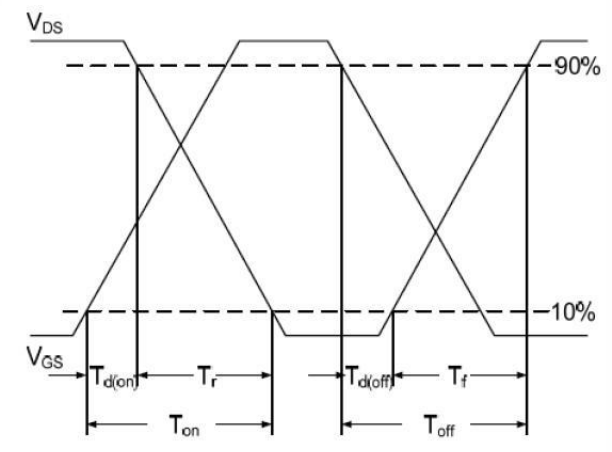


Fig.10 Switching Time Waveform

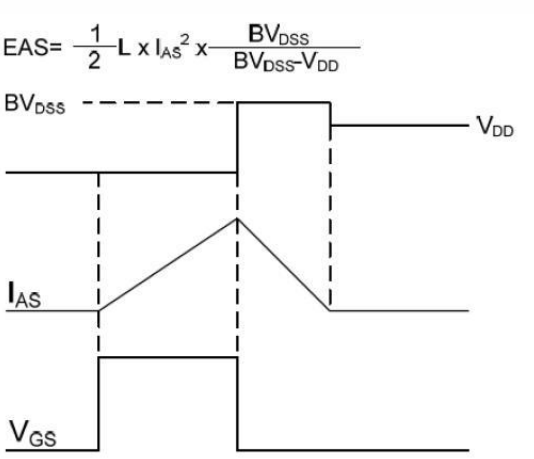


Fig.11 Unclamped Inductive Switching Wave